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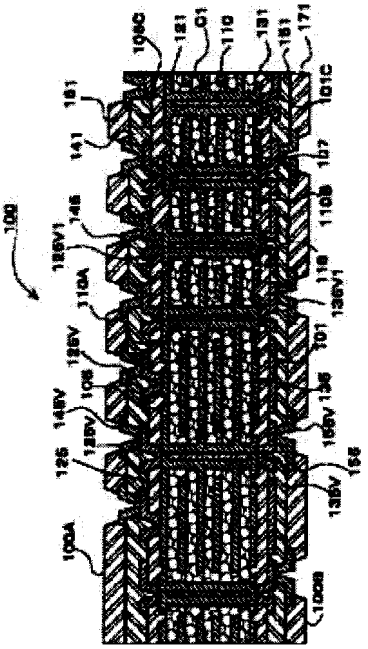
(54) WIRING BOARD, CORE BOARD, AND THEIR MANUFACTURE



(57)Abstract:

PROBLEM TO BE SOLVED: To provide a wiring board having a structure which has a capacitor built near a mounted IC chip, which is easily manufactured with high production yield, and a reduced loss in cost, even if a nonconformity of capacitor is found in a manufacturing process, a core board using the wiring board, and a method of manufacturing the core board easily at a low cost.

SOLUTION: A wiring board 100 has a core board 110, three resin insulating layers 121-171 laminated on each of the obverse and reverse surfaces 100A, 100B of the core board 110, are wiring layers 125-155 formed between the resin insulating layers. The core board 110 has a laminated capacitor C1 constituted by a plurality of complex dielectric layers 111-115, containing epoxy resin and BaTiO3 powder and a plurality of metal layer 101-106 facing and pinching these layers, and inner

metal layers 102-105 are connected to each other layer in first and second through-hole conductive bodies 107A, 107B.

[Claim(s)]
[Claim 1]A core substrate, characterized by comprising the following 1 or two or more resin insulating layers, and surface side of the above-mentioned core substrate, and the rear-face side. [which were laminated by the surface and a rear face of the above-mentioned core substrate]
A wiring layer between the above-mentioned core substrate and the above-mentioned resin insulating layer and between the above-mentioned resin insulating layers formed in either at least.
Two or more complex-dielectrics layers in which it is a wiring board which it has and the above-mentioned core substrate contains resin and high dielectric powder.
Two or more metal layers which are laminated two or more above-mentioned complex-dielectrics layers and by turns, are formed in between these layers, the undersurface of the above-mentioned complex-dielectrics layer of the bottom of the heap, and the upper surface of the above-mentioned complex-dielectrics layer of the top layer, and counter on both sides of the above-mentioned complex-dielectrics layer.
Two or more through hole conductors which are formed in a breakthrough which penetrates a complex-dielectrics layer and two or more metal layers of the above-mentioned plurality, and are prolonged to the above-mentioned core substrate surface and a core substrate rear face.
Two or more 1st through hole conductors which carry out direct continuation to the 1st inside metal layer selected every other layer from an inside metal layer by which a preparation, two or more above-mentioned complex-dielectrics layers, and two or more above-mentioned metal layers constituted a stratified capacitor, and two or more above-mentioned through hole conductors were formed between the above-mentioned layers among two or more above-mentioned metal layers.
Two or more 2nd through hole conductors which carry out direct continuation to the above-mentioned 1st through hole conductor with the connectionless 2nd inside metal layer among the above-mentioned inside metal layers.
The 3rd through hole [any / of the above-mentioned inside metal layer] conductor of plurality of non-conduction.
[Claim 2]In a core substrate, 1 or two or more resin insulating layers, and surface side of the above-mentioned core substrate, and the rear-face side, [which were laminated by the surface and a rear face of the above-mentioned core substrate] Are a wiring layer between the above-mentioned core substrate and the above-mentioned resin insulating layer and between the above-mentioned resin insulating layers formed in either at least a wiring board which it has, and the above-mentioned core substrate, A stratified capacitor which laminates by turns a central substrate, 1 or two or more complex-dielectrics layers which are formed in the surface and a rear face of this central substrate, respectively, and contain resin and high dielectric

powder, and two or more metal layers which counter on both sides of this, Two or more through hole conductors which are formed in a breakthrough which penetrates a stratified capacitor by the side of a stratified capacitor by the side of the above-mentioned surface, the above-mentioned central substrate, and the above-mentioned rear face, and are prolonged to the above-mentioned core substrate surface and a core substrate rear face, Inside of two or more above-mentioned metal layers by which a preparation and two or more above-mentioned through hole conductors are contained in a stratified capacitor by the side of the above-mentioned surface, Direct continuation is carried out to 1 or two or more metal layers which make one electrode of a surface side layer-like capacitor, Inside of two or more above-mentioned metal layers contained in the 1st through hole conductor which carries out direct continuation to 1 or two or more metal layers which make one electrode of a rear-face side layer-like capacitor among two or more above-mentioned metal layers contained in a stratified capacitor by the side of the above-mentioned rear face, and a stratified capacitor by the side of the above-mentioned surface. Direct continuation is carried out to 1 or two or more metal layers which make an electrode of another side of a surface side layer-like capacitor, The 2nd through hole conductor which carries out direct continuation to 1 or two or more metal layers which make an electrode of another side of a rear-face side layer-like capacitor among two or more above-mentioned metal layers contained in a stratified capacitor by the side of the above-mentioned rear face, A wiring board in which any of an electrode of the above-mentioned surface side layer-like capacitor and a rear-face side layer-like capacitor contain the 3rd through hole conductor of non-conduction.

[Claim 3]To IC corresponding point which is the wiring board according to claim 1 or 2, and projects a helicopter loading site of an IC chip carried in the surface of the above-mentioned wiring board among said core substrates on a thickness direction. Said 1st through hole conductor and the 2nd through hole conductor are formed among said three sorts of through hole conductors, A wiring board by which a small number of formation of said 3rd through hole conductor is carried out rather than the sum of said 1st through hole conductor which was not formed or was formed in this IC corresponding point, and the 2nd through hole conductor, and more above-mentioned 3rd through hole conductors than the above-mentioned IC corresponding point are formed in a peripheral edge part of the above-mentioned IC corresponding point.

[Claim 4]Two or more complex-dielectrics layers which are the core substrates for forming 1 or two or more resin insulating layers, and a wiring layer in the surface and rear face, and considering it as a wiring board, and contain resin and high dielectric powder, Two or more metal layers which are laminated two or more above-mentioned complex-dielectrics layers and by turns, are formed in between these layers, the undersurface of the above-mentioned complex-dielectrics layer of the bottom of the heap, and the upper surface of the above-mentioned complex-dielectrics layer of the top layer, and counter respectively on both sides of the above-mentioned complex-dielectrics layer, Two or more

through hole conductors which are formed in a breakthrough which penetrates a complex-dielectrics layer and two or more metal layers of the above-mentioned plurality, and are prolonged to the above-mentioned core substrate surface and a core substrate rear face, A preparation, two or more above-mentioned complex-dielectrics layers, and two or more above-mentioned metal layers, Constitute a stratified capacitor and two or more above-mentioned through hole conductors, The 1st through hole conductor which carries out direct continuation to the 1st inside metal layer chosen from an inside metal layer formed between the above-mentioned layers among two or more above-mentioned metal layers every other layer, The 2nd through hole conductor which carries out direct continuation to the above-mentioned 1st through hole conductor with the connectionless 2nd inside metal layer among the above-mentioned inside metal layers, and a core substrate in which any of the above-mentioned inside metal layer contain the 3rd through hole conductor of non-conduction.

[Claim 5]Form 1 or two or more resin insulating layers, and a wiring layer in the surface and rear face, are a core substrate for considering it as a wiring board, and A central substrate, A stratified capacitor which laminates by turns 1 or two or more complex-dielectrics layers which are formed in the surface and a rear face of this central substrate, respectively, and contain resin and high dielectric powder, and two or more metal layers which counter on both sides of this, Two or more through hole conductors which are formed in a breakthrough which penetrates a stratified capacitor by the side of a stratified capacitor by the side of the above-mentioned surface, the above-mentioned central substrate, and the above-mentioned rear face, and are prolonged to the above-mentioned core substrate surface and a core substrate rear face, Inside of two or more above-mentioned metal layers by which a preparation and two or more above-mentioned through hole conductors are contained in a stratified capacitor by the side of the above-mentioned surface, Direct continuation is carried out to 1 or two or more metal layers which make one electrode of a surface side layer-like capacitor, The 1st through hole conductor which carries out direct continuation to 1 or two or more metal layers which make one electrode of a rear-face side layer-like capacitor among two or more above-mentioned metal layers contained in a stratified capacitor by the side of the above-mentioned rear face, Inside of two or more above-mentioned metal layers which carry out direct continuation to 1 or two or more metal layers which make an electrode of another side of a surface side layer-like capacitor among two or more above-mentioned metal layers contained in a stratified capacitor by the side of the above-mentioned surface, and are contained in a stratified capacitor by the side of the above-mentioned rear face, A core substrate in which any of an electrode of the 2nd through hole conductor which carries out direct continuation to 1 or two or more metal layers which make an electrode of another side of a rear-face side layer-like capacitor, and the above-mentioned surface side layer-like capacitor and a rear-face side layer-like capacitor contain the 3rd through hole conductor of non-conduction.

[Claim 6]Are the core substrate according to claim 4 or 5, and in a plane direction center section of the core substrate. Said 1st through hole conductor and the 2nd through hole conductor are formed among said three sorts of through hole conductors, A core substrate by which a small number of formation of said 3rd through hole conductor is carried out rather than the sum of said 1st through hole conductor and the 2nd through hole conductor which were not formed or were formed in this center section, and many above-mentioned 3rd through hole conductors are formed in a plane direction peripheral edge part of a core substrate rather than the above-mentioned center section.

[Claim 7]A manufacturing method of a core substrate provided with two or more complex-dielectrics layers containing resin and high dielectric powder characterized by comprising the following which constitute a stratified capacitor, and two or more metal layers which counter respectively on both sides of the above-mentioned complex-dielectrics layer.

A metallic foil.

A semi-hardening complex-dielectrics layer containing resin and high dielectric powder of semi-hardening.

A three-layer film formation process of forming 3 layered films which have a reinforcement film in this order.

Three layers of patternizing film formation process of forming patternizing 3 layered film which fabricates a metallic foil of the above-mentioned 3 layered films to a prescribed pattern, and consists of a patternizing metallic foil, a semi-hardening complex-dielectrics layer, and a reinforcement film, The above-mentioned 3 layered films of 1, 1, or two or more above-mentioned patternizing 3 layered films in which the above-mentioned reinforcement film was removed, Laminate so that a semi-hardening complex-dielectrics layer and a patternizing metallic foil may lap by turns by using a metallic foil of 3 layered films of the above 1 as the bottom of the heap, and heat pressing of the metallic foil is piled up and carried out to the above-mentioned semi-hardening complex-dielectrics layer of an uppermost surface, A laminate sheet formation process which forms a laminate sheet, a through-hole formation process which forms two or more breakthroughs which penetrate a surface and rear surface of the above-mentioned laminate sheet, and a surface and rear surface metal layer formation process which a through hole conductor is formed in the above-mentioned breakthrough, and forms the surface side metal layer and the rear-face side metal layer in a surface and rear surface of the above-mentioned layered product.

[Claim 8]Are a manufacturing method of the core substrate according to claim 7, and said through-hole formation process, The 1st breakthrough that the 1st patternizing metallic foil chosen from said patternizing metallic foil every other layer exposes to inner circumference, A manufacturing method of a core substrate with which the 2nd patternizing metallic foil of the emainder which was not chosen as the above-mentioned 1st patternizing metallic foil among the above-mentioned patternizing metallic foils forms the 2nd breakthrough

exposed to inner circumference, and the 3rd breakthrough that exposes neither of the above-mentioned patternizing metallic foil to inner circumference.

[Claim 9]A complex-dielectrics layer which contains in either at least resin and high dielectric powder which constitute a stratified capacitor among the surface of a central substrate and this central substrate, and a rear face, Are two or more metal layers which counter on both sides of this a manufacturing method of a core substrate which it has, and A metallic foil, A three-layer film formation process of forming 3 layered films which have a semi-hardening complex-dielectrics layer containing resin and high dielectric powder of semi-hardening, and a reinforcement film in this order, Heat pressing of the semi-hardening complex-dielectrics layer of the above-mentioned 3 layered films in which the above-mentioned reinforcement film was removed is piled up and carried out to the above-mentioned metal layer of a central substrate which equips either with a metal layer of a prescribed pattern at least among the surface and a rear face, Form a through hole conductor a laminate sheet formation process which forms a laminate sheet, a through-hole formation process which forms two or more breakthroughs which penetrate a surface and rear surface of the above-mentioned laminate sheet, and in the above-mentioned breakthrough, and. A manufacturing method of a core substrate provided with a surface and rear surface metal layer formation process which forms the surface side metal layer and the rear-face side metal layer in a surface and rear surface of the above-mentioned laminate sheet.

[Claim 10]Two or more complex-dielectrics layers which contain in either at least resin and high dielectric powder which constitute a stratified capacitor among the surface of a central substrate characterized by comprising the following, and this central substrate, and a rear face, A manufacturing method of a core substrate provided with two or more metal layers which counter respectively on both sides of the above-mentioned complex-dielectrics layer.

A metallic foil.

A semi-hardening complex-dielectrics layer containing resin and high dielectric powder of semi-hardening.

A three-layer film formation process of forming 3 layered films which have a reinforcement film in this order.

Three layers of patternizing film formation process of forming patternizing 3 layered film which fabricates a metallic foil of the above-mentioned 3 layered films to a prescribed pattern, and consists of a patternizing metallic foil, a semi-hardening complex-dielectrics layer, and a reinforcement film, On the above-mentioned metal layer of a central substrate which equips either with a metal layer of a prescribed pattern at least among the surface and a rear face, 1 or two or more above-mentioned patternizing 3 layered films in which the above-mentioned reinforcement film was removed, It laminates so that the above-mentioned metal layer, or a patternizing metallic foil and a semi-hardening complex-dielectrics layer may lap, Heat pressing is laminated and carried out so that a semi-hardening complex-dielectrics layer of the above-

mentioned 3 layered films of 1 in which the above-mentioned reinforcement film was removed may lap on the above-mentioned patternizing metallic foil of an uppermost surface, A laminate sheet formation process which forms a laminate sheet, a through-hole formation process which forms two or more breakthroughs which penetrate a surface and rear surface of the above-mentioned laminate sheet, and a surface and rear surface metal layer formation process which a through hole conductor is formed in the above-mentioned breakthrough, and forms the surface side metal layer and the rear-face side metal layer in a surface and rear surface of the above-mentioned laminate sheet.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]About the manufacturing method of the wiring board, core substrate, and core substrate which have a core substrate, the resin insulating layer laminated by this surface and rear surface, and a wiring layer, especially, this invention builds in a capacitor and relates to the wiring board and core substrate which prevented invasion of the noise, and a manufacturing method for the same.

[0002]

[Description of the Prior Art]What forming the decoupling capacitor for noise rejection between the earth wire of an IC chip and power supply wiring is performed conventionally, for example, carries a chip capacitor in the surface, a rear face, etc. of a wiring board is used. In the wiring board 300 shown in drawing 22, laminating formation of the resin insulating layers 320, 340, and 360,330,350,370 of three layers is carried out to the surface and rear surface (figure Nakagami undersurface) of the core substrate 310, respectively, and the wiring layers 315 and 325,345,335,355 are formed between each layers. Solder SL is equipped with chip capacitor CC in the wiring layer (pad) 355 in the substrate rear (figure Nakashita side) 300B of this wiring board 300. In this wiring board 300, the two electrodes CCA and CCB of chip capacitor CC. Through each wiring layer 325 grade and the through hole conductor 316, it is pulled out to the substrate upper surface 300A 345 of the wiring board 300, i.e., a wiring layer, (pad), and is connected with the IC chip connected on the substrate upper surface 300A.

[0003]

[Problem to be solved by the invention]However, if such a chip capacitor is carried in a wiring board and it connects, the man day for it will start. Since a chip capacitor will be arranged around a substrate rear or an IC chip, the distance from an IC chip to a chip capacitor becomes long, and a noise invades into the intermediate wiring. Then, since a capacitor is moreover formed in a wiring board and one near the IC chip, it is possible to form the capacitor which used a part of resin insulating layer as the dielectric layer into a wiring board.

[0004]However, if it is going to realize by the resin insulating layer and a wiring layer, constituting from the resin insulating layer 320 and the wiring

layer 315,325 in drawing 22 etc. the structure of the capacitor which sandwiched the thin dielectric layer in the electrode layer of a large area, for example, Which short fault is easy to produce and the yield of a wiring board falls greatly. Since the fault of the formed capacitor will be discovered where it formed a resin insulating layer, a wiring layer, etc. in the core substrate and added value is attached to it, the loss amount accompanying abandonment of a fault article also becomes large.

[0005]This invention was made in view of this problem, and is . the purpose builds in a capacitor near the IC chip -- moreover -- manufacture -- it being easy and, Even if the yield is high and the fault of a capacitor is discovered in a manufacturing process, loss amount is the wiring board made into little structure and a core substrate used for such a wiring board, and providing the easy and inexpensive manufacturing method of this core substrate further.

[0006]

[Means for Solving the Problem and its Function and Effect]And 1 or two or more resin insulating layers by which the solving means was laminated by the surface and a rear face of a core substrate and the above-mentioned core substrate, Are a wiring layer between the above-mentioned core substrate and the above-mentioned resin insulating layer and between the above-mentioned resin insulating layers formed in either at least a wiring board which it has, and the above-mentioned core substrate, It laminates two or more complex-dielectrics layers containing resin and high dielectric powder, two or more above-mentioned complex-dielectrics layers, and by turns, Two or more metal layers which are formed in between these layers, the undersurface of the above-mentioned complex-dielectrics layer of the bottom of the heap, and the upper surface of the above-mentioned complex-dielectrics layer of the top layer, and counter on both sides of the above-mentioned complex-dielectrics layer, Two or more through hole conductors which are formed in a breakthrough which penetrates a complex-dielectrics layer and two or more metal layers of the above-mentioned plurality, and are prolonged to the above-mentioned core substrate surface and a core substrate rear face, A preparation, two or more above-mentioned complex-dielectrics layers, and two or more above-mentioned metal layers, Constitute a stratified capacitor and two or more above-mentioned through hole conductors, Two or more 1st through hole conductors which carry out direct continuation to the 1st inside metal layer chosen from an inside metal layer formed between the above-mentioned layers among two or more above-mentioned metal layers every other layer, and two or more 2nd through hole conductors which carry out direct continuation of the above-mentioned 1st through hole conductor to the connectionless 2nd inside metal layer among the above-mentioned inside metal layers, It is a wiring board in which any of the above-mentioned inside metal layer contain two or more 3rd through hole conductors of non-conduction.

[0007]In the wiring board of this invention, since it has the stratified capacitor constituted from a complex-dielectrics layer and a metal layer by the core substrate of these and a capacitor with big electric capacity can be arranged in

the position near electronic parts, such as an IC chip, effects, such as noise rejection, are acquired good. Since the stratified capacitor was made to build in a core substrate, the characteristic, short existence, etc. of a stratified capacitor are inspected and a wiring board can be formed for formation, i.e., a resin insulating layer, a wiring layer, etc. only using the core substrate which passed, in manufacture of a wiring board, the yield can also be made high. Since what is necessary is just to discard in the state of the core substrate in which neither the resin insulating layer nor the wiring layer is formed though the built-in capacitor has produced faults, such as a short circuit, added value can suppress the loss accompanying fault generating low. Therefore, it can be considered as an inexpensive wiring board.

[0008]And the through hole conductor which conducts the potential of the metal layer which makes the electrode of a stratified capacitor with a desired metal layer in order to enable it to take out with the rear face further, the surface of a core substrate and is formed in the core substrate. It has the 1st through hole conductor and the 2nd through hole conductor which draw the potential of the metal layer specifically located in the internal layer except the metal layer located in the core substrate surface and a rear face among two or more above-mentioned metal layers, i.e., the inner layer metal layer formed between layers, to the surface and the rear face of a core substrate. The 3rd through hole conductor which does not connect with an inner layer metal layer is also contained. Thus, in this wiring board, since three sorts of through hole conductors are prolonged even at the surface and the rear face of the core substrate, the wiring layer formed in the rear-face side of this core substrate and the wiring layer formed in the surface side are easily connectable by this through hole conductor. Therefore, if the wiring layer by the side of a rear face and other wiring boards, such as a mother board, are connected by the rear-face side and the wiring layer by the side of the surface and electronic parts, such as an IC chip, are connected by the surface side for example, other wiring boards and electronic parts are connectable through this through hole conductor.

[0009]And since a stratified capacitor is formed in parallel between the 1st through hole conductor and the 2nd through hole conductor, Electric power can be supplied to electronic parts from other wiring boards, such as a mother board, by connecting power supply wiring and grounding wiring to this 1st and 2nd through hole conductor, respectively, removing easily and certainly a noise between this power supply wiring and grounding wiring. Wiring prolonged from a metal layer of said stratified capacitor to an electronic-parts mounting surface (surface) of said wiring board is good to be characterized by including stacked beer. It is because an inductance which wiring has can be reduced by considering it as wiring as short [wiring which connects an IC chip etc. and an electrode (metal layer) of a capacitor] as possible, and thick and invasion of a noise can be controlled.

[0010]Here, what is necessary is just to choose in consideration of a dielectric constant, heat resistance, etc. as resin contained in a complex-dielectrics layer,

and resin, such as an epoxy resin, polyimide resin, and BT resin, is mentioned. Although what is necessary is just the powder of a substance which has a high dielectric constant as high dielectric powder, For example, powder of high permittivity ceramics, such as $BaTiO_3$, $PbTiO_3$, $PbZrO_3$, Pb(Ti, Zr) O_3 (what is called PZT), Pb(Mn, Nb) O_3, $SrTiO_3$, $CaTiO_3$, and $MgTiO_3$, etc. are mentioned. Since a dielectric constant of a complex-dielectrics layer is raised, metal powder, such as Ag, Au, Cu, Ag-Pd, nickel, W, and Mo, can also be included, for example.

[0011]1 or two or more resin insulating layers by which other solving means were laminated by the surface and a rear face of a core substrate and the above-mentioned core substrate, Are a wiring layer between the above-mentioned core substrate and the above-mentioned resin insulating layer and between the above-mentioned resin insulating layers formed in either at least a wiring board which it has, and the above-mentioned core substrate, A stratified capacitor which laminates by turns a central substrate, 1 or two or more complex-dielectrics layers which are formed in the surface and a rear face of this central substrate, respectively, and contain resin and high dielectric powder, and two or more metal layers which counter on both sides of this, Two or more through hole conductors which are formed in a breakthrough which penetrates a stratified capacitor by the side of a stratified capacitor by the side of the above-mentioned surface, the above-mentioned central substrate, and the above-mentioned rear face, and are prolonged to the above-mentioned core substrate surface and a core substrate rear face, Inside of two or more above-mentioned metal layers by which a preparation and two or more above-mentioned through hole conductors are contained in a stratified capacitor by the side of the above-mentioned surface, Direct continuation is carried out to 1 or two or more metal layers which make one electrode of a surface side layer-like capacitor, Inside of two or more above-mentioned metal layers contained in the 1st through hole conductor which carries out direct continuation to 1 or two or more metal layers which make one electrode of a rear-face side layer-like capacitor among two or more above-mentioned metal layers contained in a stratified capacitor by the side of the above-mentioned rear face, and a stratified capacitor by the side of the above-mentioned surface, Direct continuation is carried out to 1 or two or more metal layers which make an electrode of another side of a surface side layer-like capacitor, The 2nd through hole conductor which carries out direct continuation to 1 or two or more metal layers which make an electrode of another side of a rear-face side layer-like capacitor among two or more above-mentioned metal layers contained in a stratified capacitor by the side of the above-mentioned rear face, It is a wiring board in which any of an electrode of the above-mentioned surface side layer-like capacitor and a rear-face side layer-like capacitor contain the 3rd through hole conductor of non-conduction.

[0012]According to the wiring board of this invention, it has a stratified capacitor at the surface and the rear face of a central substrate. For this reason, since a capacitor can be arranged in the position near electronic parts,

such as an IC chip, effects, such as noise rejection, are acquired good. Since the stratified capacitor is formed in a core substrate and a wiring board can be formed only using the core substrate which inspected the characteristic, short existence, etc. of the stratified capacitor and passed, in manufacture of a wiring board, the yield can also be made high. Since what is necessary is just to discard in the state of the core substrate in which neither the resin insulating layer nor the wiring layer is formed, added value can suppress the loss accompanying fault generating low. Therefore, it can be considered as an inexpensive wiring board.

[0013]And the potential of the metal layer which makes the electrode of a stratified capacitor can be taken out with the surface and the rear face of a core substrate by the 1st through hole conductor and the 2nd through hole conductor. As for the 3rd through hole conductor of non-conduction, any of the electrode of a stratified capacitor are contained. Thus, in this wiring board, since the through hole conductor is prolonged at the surface and the rear face of the core substrate, the wiring layer formed in the rear-face side of this core substrate and the wiring layer formed in the surface side are easily connectable by this through hole conductor. Therefore, if the wiring layer by the side of a rear face and other wiring boards, such as a mother board, are connected by the rear-face side and the wiring layer by the side of the surface and electronic parts, such as an IC chip, are connected by the surface side for example, other wiring boards and electronic parts are connectable through this through hole conductor.

[0014]And since a stratified capacitor is formed in parallel between the 1st through hole conductor and the 2nd through hole conductor, Electric power can be supplied to electronic parts from other wiring boards, such as a mother board, by connecting power supply wiring and grounding wiring to this 1st and 2nd through hole conductor, respectively, removing easily and certainly a noise between this power supply wiring and grounding wiring. In this wiring board, by selecting construction material and thickness of a central substrate suitably, since a stratified capacitor is formed in the surface and a rear face of a central substrate, since a central substrate can be made to support the rigidity of a core substrate and also a wiring board, the rigidity of a wiring board is easily securable.

[0015]Although what is necessary is just to choose in consideration of an ease of heat resistance, a mechanical strength, flexibility, and processing, etc. as a central substrate, here, For example, glass fiber and epoxy resins, such as a glass cloth and a nonwoven glass fabric, A resin-resin composite material etc. which made fluororesin of the three-dimensional network structures, such as PTFE which has a glass fiber-resin composite material with resin, such as polyimide resin and BT resin, a composite material of organic fiber, such as a polyamide fiber, and resin, and a continuation stoma, impregnate resin, such as an epoxy resin, can be used. When such resin materials are used for a central substrate, it is desirable at a point which can punch a central substrate easily with a stratified capacitor by laser beam machining or drilling. A metal

plate which consists of copper, brass, nickel, aluminum, a copper-Invar copper clad, a copper-molybdenum copper clad, etc. may be used. When using these metal plates as a central substrate, structure of using a central substrate as one of the electrodes of a capacitor can also be adopted. Wiring prolonged from a metal layer of said stratified capacitor to an electronic-parts mounting surface (surface) of said wiring board is good to be characterized by including stacked beer. It is because an inductance which wiring has can be reduced by considering it as wiring as short [wiring which connects an IC chip etc. and an electrode (metal layer) of a capacitor] as possible, and thick and invasion of a noise can be controlled.

[0016]To one of the above, are a wiring board of a description and said two or more through hole conductors, It is preferred to consider it as the wiring board which an inside is filled up with a plug material, equips said core substrate surface and a core substrate rear face with an occlusion part, respectively, and is provided with the occlusion part top beer conductor which penetrates said resin insulating layer laminated by the surface of the above-mentioned core substrate among the above-mentioned occlusion parts on the surface side occlusion part by the side of the above-mentioned core substrate surface.

[0017]By thus, the thing for which it is filled up with a plug material, an occlusion part is formed, and an occlusion part top beer conductor is formed in a through hole conductor. Through a through hole conductor, it is a shorter distance, therefore the electrode of a stratified capacitor can be drawn to the wiring board surface with low resistance and a low inductance, and invasion of a noise can be prevented further.

[0018]It is the above-mentioned wiring board and it is preferred to consider it as the wiring board which accumulates a beer conductor on said occlusion part top beer conductor further. Thus, if it is the structure of stacked beer of accumulating a beer conductor on an occlusion part top beer conductor further, the direct continuation of an occlusion part top beer conductor and the beer conductor on it can be carried out. Therefore, through a through hole conductor, it is a still shorter distance, therefore the electrode of a stratified capacitor can be further drawn to the wiring board surface with low resistance and a low inductance, and invasion of a noise can be prevented.

[0019]To IC corresponding point which is the above-mentioned wiring board and projects the helicopter loading site of the IC chip carried in the surface of the above-mentioned wiring board among said core substrates on a thickness direction. Said 1st through hole conductor and the 2nd through hole conductor are formed among said three sorts of through hole conductors, A small number of formation of said 3rd through hole conductor is carried out rather than the sum of said 1st through hole conductor which was not formed or was formed in this IC corresponding point, and the 2nd through hole conductor, It is good for the peripheral edge part of the above-mentioned IC corresponding point for the above-mentioned 3rd through hole conductor to consider it as the wiring board currently formed more mostly than the above-mentioned IC corresponding point.

[0020]As for the electrode or power supply wiring, and grounding wiring of the capacitor formed in the power supply terminal, earth terminal, and wiring board of an IC chip, as mentioned above, connecting in the shortest possible distance is desirable. It is for preventing invasion of a noise for wiring as low resistance and a low inductance. On the other hand, it is not called for that the signal wiring linked to a signal terminal is low resistance and a low inductance like connection with a capacitor, power supply wiring, and grounding wiring.

[0021]On the other hand, in the wiring board of this invention, more 3rd through hole conductors to the peripheral edge part used for signal wiring etc. than IC corresponding point are formed. That is, many 3rd through hole conductors are formed in the peripheral edge part of IC corresponding point. For this reason, in IC corresponding point located directly under an IC chip, in forming the 1st through hole conductor and the 2nd through hole conductor, there is no necessity of taking arrangement into consideration, or necessity decreases the 3rd through hole conductor. Therefore, the 1st through hole conductor and the 2nd through hole conductor can be arranged in a suitable position, and between these, and the power supply terminals of an IC chip and earth terminals can be connected with a very short distance. Thereby, resistance between the 1st and 2nd through hole conductor, and the power supply terminal of an IC chip and an earth terminal and an inductance can be made as low as possible, and the noise which invades in this portion can be reduced. In this wiring board, since the stratified capacitor is formed between the 1st and 2nd through hole conductors, a noise can be reduced also with this point. It is still more preferred for all the 3rd through hole conductors to be formed in the peripheral edge part of IC corresponding point, to make it not form the 3rd through hole conductor in IC corresponding point, and to do in this way so that he can understand easily from the above.

[0022]Two or more complex-dielectrics layers which other solving means are the core substrates for forming 1 or two or more resin insulating layers, and a wiring layer in the surface and rear face, and considering it as a wiring board, and contain resin and high dielectric powder, Two or more metal layers which are laminated two or more above-mentioned complex-dielectrics layers and by turns, are formed in between these layers, the undersurface of the above-mentioned complex-dielectrics layer of the bottom of the heap, and the upper surface of the above-mentioned complex-dielectrics layer of the top layer, and counter respectively on both sides of the above-mentioned complex-dielectrics layer, Two or more through hole conductors which are formed in a breakthrough which penetrates a complex-dielectrics layer and two or more metal layers of the above-mentioned plurality, and are prolonged to the above-mentioned core substrate surface and a core substrate rear face (the undersurface of a complex-dielectrics layer of the bottom of the heap, and upper surface of a complex-dielectrics layer of the above-mentioned top layer), A preparation, two or more above-mentioned complex-dielectrics layers, and two or more above-mentioned metal layers, Constitute a stratified capacitor

and two or more above-mentioned through hole conductors, The 1st through hole conductor which carries out direct continuation to the 1st inside metal layer chosen from an inside metal layer formed between the above-mentioned layers among two or more above-mentioned metal layers every other layer, The above-mentioned 1st through hole conductors are the 2nd through hole conductor which carries out direct continuation to the connectionless 2nd inside metal layer, and a core substrate in which any of the above-mentioned inside metal layer contain the 3rd through hole conductor of non-conduction among the above-mentioned inside metal layers.

[0023]According to this invention, by having made the capacitor which is easy to produce faults, such as a short circuit, build in a core substrate, when a core substrate is completed, electric capacity, short existence, etc. of a stratified capacitor can be judged. Therefore, since only the core substrate which passed the predetermined standard can be used in forming a wiring board, the yield of the whole wiring board can be made high. Since the case where which fault with poor short circuit and capacity of a stratified capacitor is discovered and discarded where it formed the resin insulating layer and the wiring layer and added value is attached can be lessened, loss amount can also be controlled.

[0024]And in order to be able to connect easily the potential of the metal layer which makes the electrode of a stratified capacitor with the surface of a core substrate, and the wiring layer which is further taken out with the rear face and is formed in the surface [of a core substrate], and rear-face side, the predetermined inside metal layer and the through hole conductor to conduct are formed in the core substrate. It has the 1st through hole conductor and the 2nd through hole conductor which draw the potential of the metal layer specifically located in the internal layer except the metal layer located in the core substrate surface and a rear face among two or more above-mentioned metal layers, i.e., the inner layer metal layer formed between layers, to the surface and the rear face of a core substrate. The 3rd through hole conductor which does not connect with an inner layer metal layer is also contained. Thus, in this core substrate, since three sorts of through hole conductors are prolonged even at the surface and the rear face of the core substrate, respectively, the wiring layer formed in the rear-face side of this core substrate and the wiring layer formed in the surface side are easily connectable by this through hole conductor. And since a stratified capacitor is formed in parallel between the 1st through hole conductor and the 2nd through hole conductor, the noise between this power supply wiring and grounding wiring is easily and certainly removable by connecting power supply wiring and grounding wiring to this 1st and 2nd through hole conductor, respectively.

[0025]Form 1 or two or more resin insulating layers, and a wiring layer in the surface and rear face, and the solving means of further others is a core substrate for considering it as a wiring board, and A central substrate, The stratified capacitor which laminates by turns 1 or two or more complex-dielectrics layers which are formed in the surface and the rear face of this central substrate, respectively, and contain resin and high dielectric powder,

and two or more metal layers which counter on both sides of this, Two or more through hole conductors which are formed in the breakthrough which penetrates the stratified capacitor by the side of the stratified capacitor by the side of the above-mentioned surface, the above-mentioned central substrate, and the above-mentioned rear face, and are prolonged to the above-mentioned core substrate surface and a core substrate rear face, The inside of two or more above-mentioned metal layers by which a preparation and two or more above-mentioned through hole conductors are contained in the stratified capacitor by the side of the above-mentioned surface, Direct continuation is carried out to 1 or two or more metal layers which make one electrode of a surface side layer-like capacitor, The 1st through hole conductor which carries out direct continuation to 1 or two or more metal layers which make one electrode of a rear-face side layer-like capacitor among two or more above-mentioned metal layers contained in the stratified capacitor by the side of the above-mentioned rear face, The inside of two or more above-mentioned metal layers which carry out direct continuation to 1 or two or more metal layers which make the electrode of another side of a surface side layer-like capacitor among two or more above-mentioned metal layers contained in the stratified capacitor by the side of the above-mentioned surface, and are contained in the stratified capacitor by the side of the above-mentioned rear face, It is a core substrate in which any of the electrode of the 2nd through hole conductor which carries out direct continuation to 1 or two or more metal layers which make the electrode of another side of a rear-face side layer-like capacitor, and the above-mentioned surface side layer-like capacitor and a rear-face side layer-like capacitor contain the 3rd through hole conductor of non-conduction.

[0026]According to the core substrate of this invention, it has a stratified capacitor at the surface and a rear face of a central substrate. For this reason, since a capacitor can be arranged in a position near electronic parts, such as an IC chip, effects, such as noise rejection, are acquired good. Since a stratified capacitor is formed in a core substrate and a wiring board can be formed only using a core substrate which inspected the characteristic, short existence, etc. of a stratified capacitor and passed, in manufacture of a wiring board, a yield can also be made high. Since what is necessary is just to discard in the state of a core substrate in which neither a resin insulating layer nor a wiring layer is formed though a stratified capacitor has produced faults, such as a short circuit, added value can suppress a loss accompanying fault generating low. And in this core substrate, since three sorts of through hole conductors are prolonged even at the surface and a rear face of a core substrate, respectively, a wiring layer formed in the rear-face side of this core substrate and a wiring layer formed in the surface side are easily connectable by this through hole conductor.

[0027]It is the above-mentioned core substrate and, as for said central substrate, it is preferred to consider it as a core substrate thicker than said complex-dielectrics layer. Thus, if a central substrate is made thicker than a complex-dielectrics layer, the rigidity of a central substrate becomes high, and

the core substrate can make a central substrate able to support the rigidity of a wiring board which used this, and can use it as an easy core substrate and a wiring board of handling.

[0028]It is the above-mentioned core substrate and, as for said complex-dielectrics layer and metal layer which were formed in the surface side of said central substrate, and said complex-dielectrics layer and metal layer which were formed in the rear-face side of said central substrate, it is preferred that a number of layers, construction material, and the thickness of a corresponding each layer consider it as the core substrate made equal. In the surface [of a central substrate], and rear-face side, when the thickness of the number of layers of a complex-dielectrics layer or a metal layer, construction material, and a corresponding each layer differs, a coefficient of thermal expansion, the contraction in the case of core substrate formation, etc. may become imbalanced by both sides of a central substrate, and curvature may arise in a core substrate. In this invention, since thickness of a number of layers, construction material, and a corresponding each layer is made equal, curvature of a core substrate is not produced and it can be considered as the core substrate of the stable form.

[0029]It is the above-mentioned core substrate and, as for said two or more through hole conductors, it is preferred to consider it as the core substrate which an inside is filled up with a plug material and equips said core substrate surface and a core substrate rear face with an occlusion part, respectively. If the occlusion part is formed in the through hole conductor, a beer conductor (occlusion part top beer conductor) can be further formed on this occlusion part. Since a wiring layer will not intervene between a through hole conductor and a beer conductor but both will do direct continuation if this occlusion part top beer conductor is formed, it is realizable with low resistance and wiring of a low inductance.

[0030]To one of the above, are a core substrate of a description and in the plane direction center section of the core substrate. Said 1st through hole conductor and the 2nd through hole conductor are formed among said three sorts of through hole conductors, A small number of formation of said 3rd through hole conductor is carried out rather than the sum of said 1st through hole conductor which was not formed or was formed in this center section, and the 2nd through hole conductor, The above-mentioned 3rd through hole conductor is better for the plane direction peripheral edge part of a core substrate than the above-mentioned center section to consider it as the core substrate currently formed. [many]

[0031]When it carries an IC chip in a wiring board, generally an IC chip is carried in the center section of the wiring board. By the way, as for the capacitor formed in the power supply terminal, earth terminal, and wiring board of an IC chip or power supply wiring, or grounding wiring, as mentioned above, connecting in the shortest possible distance is desirable. It is for preventing invasion of a noise for wiring as low resistance and a low inductance. On the other hand, it is not called for that the signal wiring linked

to a signal terminal is low resistance and a low inductance like a capacitor, power supply wiring, and grounding wiring.

[0032]On the other hand, in the core substrate of this invention, more 3rd through hole conductors to the peripheral edge part used for signal wiring etc. than a center section are formed. That is, many 3rd through hole conductors are formed in the peripheral edge part. For this reason, in the center section located directly under an IC chip, in forming the 1st through hole conductor and the 2nd through hole conductor, there is no necessity of taking arrangement into consideration, or necessity decreases the 3rd through hole conductor. Therefore, the 1st through hole conductor and the 2nd through hole conductor can be arranged in a suitable position, and between these, and the power supply terminals of an IC chip and earth terminals can be connected with a very short distance. Resistance between the 1st and 2nd through hole conductor, and the power supply terminal of an IC chip and earth terminal linked to each electrode of a stratified capacitor and an inductance can be made as low as possible by this, and the noise which invades in this portion can be reduced.

[0033]1 or two or more complex-dielectrics layers containing resin and high dielectric powder in which a solving means of further others constitutes a stratified capacitor, Are two or more metal layers which counter respectively on both sides of the above-mentioned complex-dielectrics layer a manufacturing method of a core substrate which it has, and A metallic foil, A three-layer film formation process of forming 3 layered films which have a semi-hardening complex-dielectrics layer containing resin and high dielectric powder of semi-hardening, and a reinforcement film in this order, Three layers of patternizing film formation process of forming patternizing 3 layered film which fabricates a metallic foil of the above-mentioned 3 layered films to a prescribed pattern, and consists of a patternizing metallic foil, a semi-hardening complex-dielectrics layer, and a reinforcement film, The above-mentioned 3 layered films of 1, 1, or two or more above-mentioned patternizing 3 layered films in which the above-mentioned reinforcement film was removed, Laminate so that a semi-hardening complex-dielectrics layer and a patternizing metallic foil may lap by turns by using a metallic foil of 3 layered films of the above 1 as the bottom of the heap, and heat pressing of the metallic foil is piled up and carried out to the above-mentioned semi-hardening complex-dielectrics layer of an uppermost surface, Form a through hole conductor a laminate sheet formation process which forms a laminate sheet, a through-hole formation process which forms two or more breakthroughs which penetrate a surface and rear surface of the above-mentioned laminate sheet, and in the above-mentioned breakthrough, and. It is a manufacturing method of a core substrate provided with a surface and rear surface metal layer formation process which forms the surface side metal layer and the rear-face side metal layer in a surface and rear surface of the above-mentioned layered product.

[0034]In the manufacturing method of the core substrate of this invention, 3

layered films and patternizing 3 layered film are formed beforehand, the 3 layered films, patternizing 3 layered film, and metallic foil which removed the reinforcement film with the laminate sheet formation process are laminated in order, heat pressing is carried out, and a laminate sheet is formed at once. Therefore, it is not necessary to form one layer of complex-dielectrics layers and metal layers at a time in order like [in the case of forming a build-up multilayer interconnection board]. Since 3 layered films and patternizing 3 layered film are formed independently beforehand, it laminates and a laminate sheet can be formed at once, a core substrate production process becomes simply and short, and can manufacture a core substrate inexpensive. Since the 3 layered films and patternizing 3 layered film which have a reinforcement film were used, handling of a complex-dielectrics layer, a metallic foil, or a patternizing metallic foil -- since it is easy, and workability is good even when a metallic foil and semi-hardening complex-dielectrics layer thickness are made thin even if, a core substrate can be manufactured easily. Since the semi-hardening complex-dielectrics layer is covered with the reinforcement film, garbage etc. can be prevented also from adhering to the semi-hardening complex-dielectrics layer in the state where it is adhesive for semi-hardening, and fault generating by garbage can also be prevented.

[0035]In the manufacturing method of said core substrate here said three-layer film formation process, It is good to consider it as the manufacturing method of the core substrate applying to said metallic foil the complex-dielectrics paste containing said resin and high dielectric powder, sticking and heating a reinforcement film in an unhardened complex-dielectrics layer, carrying out semi-hardening of the above-mentioned resin, and forming said 3 layered films. In order to apply a complex-dielectrics paste to a metallic foil, it is a stage of 3 layered films, or also after considering it as a laminate sheet, it is because the adhesion of a metallic foil, a patternizing metallic foil, and a complex-dielectrics layer becomes good. Since neither air nor garbage can enter easily among both, generating of fault can also be prevented.

[0036]Adhesives may be used when laminating. Namely, in a manufacturing method of said core substrate said laminate sheet formation process, It is good also as a manufacturing method of a core substrate which laminates a semi-hardening complex-dielectrics layer and a patternizing metallic foil by using a metallic foil of said 3 layered films of 1 as the bottom of the heap so that it may lap by turns via an adhesives layer, puts a metallic foil on said semi-hardening complex-dielectrics layer of an uppermost surface via an adhesives layer, and is characterized by carrying out heat pressing. It is because it can be considered as a complex-dielectrics layer and a layered product on which a metallic foil was pasted up certainly if it does in this way. On the other hand, when it laminates without passing an adhesives layer, electric capacity of a stratified capacitor can be enlarged as compared with a case where adhesives are used.

[0037]Are a manufacturing method of the above-mentioned core substrate, and said through-hole formation process, The 1st breakthrough that the 1st

patternizing metallic foil chosen from said patternizing metallic foil every other layer exposes to inner circumference, It is good for the 2nd patternizing metallic foil of the emainder which was not chosen as the above-mentioned 1st patternizing metallic foil among the above-mentioned patternizing metallic foils to consider it as a manufacturing method of a core substrate which forms the 2nd breakthrough exposed to inner circumference, and the 3rd breakthrough that neither of the above-mentioned patternizing metallic foil exposes to inner circumference.

[0038]Thus, when three sorts of through hole conductors are formed, it is because it will be in the state where the 1st patternizing metallic foil and the 2nd patternizing metallic foil countered on both sides of a complex-dielectrics layer, every other layer and a laminated stratified capacitor can be formed easily.

[0039]1 or two or more complex-dielectrics layers to which the solving means of further others contains in either at least resin and the high dielectric powder which constitute a stratified capacitor among the surface of a central substrate and this central substrate, and a rear face, Are two or more metal layers which counter on both sides of this a manufacturing method of the core substrate which it has, and A metallic foil, The three-layer film formation process of forming the 3 layered films which have a semi-hardening complex-dielectrics layer containing resin and the high dielectric powder of semi-hardening, and a reinforcement film in this order, Heat pressing of the semi-hardening complex-dielectrics layer of the above-mentioned 3 layered films in which the above-mentioned reinforcement film was removed is piled up and carried out to the above-mentioned metal layer of the central substrate which equips either with the metal layer of a prescribed pattern at least among the surface and a rear face, Form a through hole conductor the laminate sheet formation process which forms a laminate sheet, the through-hole formation process which forms two or more breakthroughs which penetrate the surface and rear surface of the above-mentioned laminate sheet, and in the above-mentioned breakthrough, and. It is a manufacturing method of a core substrate provided with the surface and rear surface metal layer formation process which forms the surface side metal layer and the rear-face side metal layer in the surface and rear surface of the above-mentioned laminate sheet.

[0040]In the manufacturing method of the core substrate of this invention, 3 layered films are formed beforehand, heat pressing of the 3 layered films from which the reinforcement film was removed with the laminate sheet formation process is laminated and carried out to either at least among the surface and rear surfaces of a central substrate, and a laminate sheet is formed at once. Therefore, it is not necessary to form one layer of complex-dielectrics layers and metal layers in the surface and the rear face of a central substrate at a time in order like [in the case of forming a build-up multilayer interconnection board]. Since 3 layered films are formed independently beforehand, it laminates and a laminate sheet can be formed at once, a core substrate production process becomes simply and short, and can manufacture a core

substrate inexpensive. moreover -- since the 3 layered films which have a reinforcement film were used -- handling of a complex-dielectrics layer or a metal layer -- since it is easy, and workability is good even when a metallic foil and complex-dielectrics (semi-hardening) layer thickness are made thin even if, a core substrate can be manufactured easily. Since the semi-hardening complex-dielectrics layer is covered with the reinforcement film, garbage etc. can be prevented also from adhering to the semi-hardening complex-dielectrics layer in the state where it is adhesive for semi-hardening, and fault generating by garbage can also be prevented.

[0041]In the manufacturing method of said core substrate here said three-layer film formation process, It is good to consider it as the manufacturing method of the core substrate applying to said metallic foil the complex-dielectrics paste containing said resin and high dielectric powder, sticking and heating a reinforcement film in an unhardened complex-dielectrics layer, carrying out semi-hardening of the above-mentioned resin, and forming said 3 layered films. In order to apply a complex-dielectrics paste to a metallic foil, it is a stage of 3 layered films, or also after considering it as a laminate sheet, it is because the adhesion of a metallic foil and a complex-dielectrics layer becomes good. Since neither air nor garbage can enter easily among both, generating of fault can also be prevented.

[0042]Two or more complex-dielectrics layers to which other solving means contain in either at least resin and the high dielectric powder which constitute a stratified capacitor among the surface of a central substrate and this central substrate, and a rear face, Are two or more metal layers which counter respectively on both sides of the above-mentioned complex-dielectrics layer a manufacturing method of the core substrate which it has, and A metallic foil, The three-layer film formation process of forming the 3 layered films which have a semi-hardening complex-dielectrics layer containing resin and the high dielectric powder of semi-hardening, and a reinforcement film in this order, Three layers of patternizing film formation process of forming the patternizing 3 layered film which fabricates the metallic foil of the above-mentioned 3 layered films to a prescribed pattern, and consists of a patternizing metallic foil, a semi-hardening complex-dielectrics layer, and a reinforcement film, On the above-mentioned metal layer of the central substrate which equips either with the metal layer of a prescribed pattern at least among the surface and a rear face, 1 or two or more above-mentioned patternizing 3 layered films in which the above-mentioned reinforcement film was removed, The laminate sheet formation process which laminates so that the above-mentioned metal layer, or a patternizing metallic foil and a semi-hardening complex-dielectrics layer may lap, laminates and carries out heat pressing so that the semi-hardening complex-dielectrics layer of the above-mentioned 3 layered films of 1 in which the above-mentioned reinforcement film was removed on the above-mentioned patternizing metallic foil of an uppermost surface may lap, and forms a laminate sheet, It is a manufacturing method of a core substrate provided with the through-hole formation process which forms two or more

breakthroughs which penetrate the surface and rear surface of the above-mentioned laminate sheet, and the surface and rear surface metal layer formation process which a through hole conductor is formed in the above-mentioned breakthrough, and forms the surface side metal layer and the rear-face side metal layer in the surface and rear surface of the above-mentioned laminate sheet.

[0043]In the manufacturing method of the core substrate of this invention, 3 layered films and patternizing 3 layered film are formed beforehand, Heat pressing of the patternizing 3 layered film and 3 layered films which removed the reinforcement film is laminated and carried out to either at least among the surface of a central substrate, and a rear face with a laminate sheet formation process, and a laminate sheet is formed at once. Therefore, it is not necessary to form one layer of complex-dielectrics layers and metal layers in the surface and the rear face of a central substrate at a time in order like [in the case of forming a build-up multilayer interconnection board]. Since 3 layered films and patternizing 3 layered film are formed independently beforehand, it laminates and a laminate sheet can be formed at once, a core substrate production process becomes simply and short, and can manufacture a core substrate inexpensive. Since the 3 layered films and patternizing 3 layered film which removed the reinforcement film were laminated, electric capacity of the stratified capacitor formed can be enlarged.

[0044]moreover -- since the 3 layered films and patternizing 3 layered film which have a reinforcement film were used -- handling of a complex-dielectrics layer or a metal layer -- since it is easy, and workability is good even when a metallic foil and semi-hardening complex-dielectrics layer thickness are made thin even if, a core substrate can be manufactured easily. Since the semi-hardening complex-dielectrics layer is covered with the reinforcement film, garbage etc. can be prevented also from adhering to the semi-hardening complex-dielectrics layer in the state where it is adhesive for semi-hardening, and fault generating by garbage can also be prevented.

[0045]

[Mode for carrying out the invention](Embodiment 1) It ranks second and the embodiment of the core substrate and wiring board concerning this invention, and a manufacturing method for the same is described with Drawings. The core substrate 110 shown in drawing 1 is laminated the five-layer complex-dielectrics layers 111-115, these complex-dielectrics layer 111 grade, and by turns, It has the metal layers 101-106 which consist of Cu formed in between the layer, the figure Nakashita side of the complex-dielectrics layer 111, and the figure Nakagami side of the complex-dielectrics layer 115, respectively, and the through hole conductor 107 which is formed in the inner skin of the breakthrough H and similarly consists of Cu(s). The complex-dielectrics layer 111 grade and the metal layer 101 grade which counters via these constitute the stratified capacitor C1 which has a dielectric layer of five layers. What (for example, the metal layers 103 and 105, or 102 and 104) is made into common electric potential among each inside metal layers (inside metal layer) 102-105,

For example, conduction is carried out to the metal layer 101,106 on the core substrate surface 110A or the rear face 110B of a core substrate by the 1st through hole conductor 107A or the 2nd through hole conductor 107B, respectively. That is, direct continuation of the 1st inside metal layer 102,104 chosen every other layer among inside metal layers is carried out to the 1st through hole conductor 107A. On the other hand, direct continuation of the 2nd inside metal layer 103,105 which was not chosen is carried out to the 2nd through hole conductor 107B. It is used as an electrode which constitutes the stratified capacitor C1, and also the outside metal layer 101,106 is used as a wiring layer.

[0046]Like the 3rd through hole conductor 107C, in order to use for signal wiring etc., there are some which are not conducted in the through hole conductor 107 with internal metal layer 102 grade. In this core substrate 110, as described above, a part of metal layers 102 and 104 and metal layers 101 and 106 have conducted mutually, and on the other hand, a part of metal layers 103 and 105 and metal layers 101 and 106 have conducted mutually. Therefore, these metal layers are making the stratified capacitor C1 by countering on both sides of each complex-dielectrics layer 111 grade.

[0047]And three sorts of through hole conductors 107A, 107B, and 107C, Since it has extended to the surface 110A and the rear face 110B of the core substrate 110, a wiring layer formed in the rear-face 110B side of the core substrate 110 and a wiring layer formed in the surface 110A side are connectable via these through hole conductors 107. Here, since it means inserting the stratified capacitor C1 in parallel between power supply potential and earth potentials when the 1st through hole conductor 107A is connected to power supply wiring and the 2nd through hole conductor 107B is connected to grounding wiring, for example, a noise on which such potential is overlapped is absorbable. On the other hand, if it is connected with the 3rd through hole conductor 107C, signal wiring is in a state divorced from the stratified capacitor C1, and can let inside of the core substrate 110 pass.

[0048]It is what each of complex-dielectrics layer 111 grades shall be 50 micrometers in thickness, and consists $BaTio_3$ powder of a ceramic metal-resin composite material which distributed 30vol% and Cu powder in an epoxy resin 20vol%, A dielectric constant is made higher than usual resin by mixing of $BaTio_3$ powder of high permittivity (specific-inductive-capacity epsilonr= about 18000), and Cu powder (epsilonr=30). For this reason, let electric capacity of the stratified capacitor C1 which the core substrate 110 constitutes (built-in) be a comparatively big value (electric capacity 3.0nF).

[0049]Subsequently, the wiring board 100 is explained. The wiring board 100 shown in drawing 2 forms in the surface and rear surfaces 110A and 110B of this core substrate 110 the two-layer wiring layer 125,145,135,155 which consists of the resin insulating layers 121, 141, and 161,131,151,171 of three layers which consist of epoxy resins, respectively, and Cu. Each wiring layer 125 grade is formed between layers of resin insulating layer 121 grade, and it contains the beer conductors 125V, 145V, 135V, and 155V for connecting with a

metal layer and a wiring layer which are located in a lower layer. An inside of the through hole conductor 107 of the core substrate 110 is filled up with the plug material 116 which consists of epoxy resins, respectively, and it is closed by the occlusion parts 101C and 106C formed in the metal layer 101,106, respectively.

[0050]This wiring board 100 builds in the stratified capacitor C1 formed in the core substrate 110, and can connect an IC chip (not shown) and a stratified capacitor which are carried in the wiring board surface (IC chip mounting surface) 100A in a very near distance so that he can understand easily from the above-mentioned explanation. Therefore, noise rejection can be performed certainly. Signal wiring can be designed and taken about with the same line width as usual among the wiring layers 125,145,135,155 which form the resin wiring layer 121,141 grade itself between layers of resin insulating layer 121 grade unlike a case where it is considered as a thing of high permittivity. It is because the same epoxy resin as usual can be used for resin insulating layer 121 grade, so these dielectric constants do not change to it, therefore impedance of signal wiring does not change to it, either. Therefore, a design of a signal wiring layer wiring layer, etc. can be made easy.

[0051]The occlusion parts 101C and 106C are formed, and occlusion part top beer conductor 125V1,135V1 which carries out direct continuation to this occlusion part is formed on this occlusion part 101C and 106C, respectively. Since the through hole conductor 107 and occlusion part top beer conductor 125V1,135V1 are connectable in a very short distance if it does in this way, resistance and an inductance which wiring layer 125 grade has can be reduced. Therefore, especially, wiring between the stratified capacitor C1 and an IC chip is shortened, and it is useful to prevent invasion of a noise as low resistance and a low inductance.

[0052]Subsequently, the manufacturing method of the above-mentioned core substrate 110 is explained. First, a three-layer film formation process is explained. As shown in drawing 3 (a), it is a 10-100-micrometer-thick range (in this example.) about the complex-dielectrics paste which prepared the 18-micrometer-thick copper foil 11, and made the upper surface 11A distribute the powder and Cu powder of $BaTio_3$ to epoxy resin paste. It applies to about 60 micrometers and the unhardened complex-dielectrics layer 12C is formed. Then, in order to raise viscosity, maintaining surface adhesiveness, desiccation for 50 x 60 minutes is performed.

[0053]Subsequently, reinforcement film RF which consists of 200-micrometer-thick polyimide or polyester is stuck on the surface 12A of an unhardened complex-dielectrics layer, it heats on the conditions for 80 x 60 minutes, and the copper foil 11, the complex-dielectrics layer 12 of a semi hardened state, and the 3 layered films 10 that have reinforcement film RF in this order are formed. Since these 3 layered films 10 are reinforced with reinforcement film RF, Since it will have the rigidity which is equal to the handling in each process even if the thickness of the copper foil 11 and the patternizing copper foil 21 and 31 mentioned later, or the semi-hardening complex-dielectrics layer

12 is thin, handling is easy, A core substrate with thin metal layer 101 grade and thin complex-dielectrics layer 111 grade as shown in drawing 1 can be formed easily. In these 3 layered films 10, since it has structure which sandwiched the adhesive semi-hardening complex-dielectrics layer 12 with the copper foil 11 and reinforcement film RF, dust is prevented also from adhering to the semi-hardening complex-dielectrics layer 12. Since the complex-dielectrics paste was applied and the unhardened complex-dielectrics layer 12C was formed on the copper foil 11 in these 3 layered films 10, neither air nor dust intervenes between the copper foil 11 and the semi-hardening complex-dielectrics layer 12, and both adhesion is good. It is more desirable when the upper surface 11A of the copper foil 11 is beforehand roughened with techniques, such as blackening treatment, needlelike plating, and roughening etching, in order to raise these both adhesion further.

[0054]Subsequently, three layers of patternizing film formation process is explained. As shown in drawing 4 (a), dry film DF is stuck on the exposed surface 11B (figure Nakagami side) of the copper foil 11 among these 3 layered films 10, exposure development is carried out, and the opening DFO of a prescribed pattern is formed. Subsequently, as shown in drawing 4 (b), the copper foil 11 is etched, it is considered as the 1st patternizing copper foil 21 of a prescribed pattern, dry film DF is exfoliated, and the 1st patternizing 3 layered film 20 is formed. Similarly, as shown in drawing 4 (c), the 2nd patternizing 3 layered film 30 which has the 2nd patternizing copper foil 31 which is different in the 1st patternizing 3 layered film 20 is also formed. In a laminate sheet formation process which following-, when it laminates, in order to raise adhesion with the adjacent semi-hardening complex-dielectrics layer 12, when an exposed surface of the patternizing copper foil 21 and 31 is beforehand roughened with techniques, such as blackening treatment, needlelike plating, and roughening etching, it is more desirable.

[0055]Then, in a laminate sheet formation process, as shown in drawing 5 (a), the copper foil 11 of the bilayer film 10C which removed reinforcement film RF among the 3 layered films 10 shown in drawing 3 (b) is turned down (bottom of the heap), The 1st and 2nd patternizing bilayer films 20C and 30C which similarly removed reinforcement film RF of the 1st and 2nd patternizing 3 layered films 20 and 30, respectively are laminated in order. Specifically, it laminates so that the semi-hardening complex-dielectrics layer 12 and the patternizing copper foil 21 and 31 may lap by turns. In this embodiment, the 1st patternizing bilayer film 20C and the 2nd patternizing bilayer film 30C were laminated every [two-layer one] and by turns, respectively. And the 18-micrometer-thick copper foil 41 is piled up on the semi-hardening complex-dielectrics layer 12 of an uppermost surface, in a vacuum, heat pressing is carried out to figure Nakagami down on condition of 180 x2Hr and 30 kg/cm^2, an epoxy resin of a complex-dielectrics layer is stiffened, and the layered product 50 shown in drawing 5 (b) is formed at once. The five-layer complex-dielectrics layers 111-115 and the metal layers 102-105 of a prescribed pattern are laminated by turns, and this layered product 50 has the copper foil 11 and

41 in those surface and rear surfaces 50A and 50B.
[0056]Then, in a through-hole formation process, as shown in drawing 6, the surface and rear surface 50A of this laminate sheet 50 and the breakthrough H with a diameter of 60 micrometers which penetrates between 50B are punched in a specified position using the 4th harmonics of an YAG laser. What the end faces 102H and 104H of metal layer 102 grade, or 103H and 105H expose is formed in inner skin of the punched breakthrough H. That is, inside of the patternizing metallic foils 21 and 31 used as the inner layer metal layers 102-105, The 1st breakthrough H1 that the 1st patternizing metallic foils 21 and 21 selected every other layer expose to inner circumference, the 2nd breakthrough H2 that the 2nd patternizing metal layers 31 and 31 which were not chosen expose to inner circumference, and the 3rd breakthrough H3 that exposes neither of the patternizing metal layers, 21 nor 31, are formed. In consideration of an aperture, construction material of a laminate sheet, etc., the 3rd harmonics of an YAG laser, a CO2 laser, or a drill may perform punching.
[0057]In a surface and rear surface metal layer formation process, the through hole conductor 107 is formed with the publicly known PTH formation technique in the breakthrough H, and using the copper foil 11 and 41, the metal layer 101,106 of a prescribed pattern is formed and the core substrate 110 is completed (refer to drawing 1). Metal layer 102 grade among [107A and 107B] the through hole conductors 107 (for example, the 1st and 2nd through hole conductors), Since it conducts in end-face 102H grade, as mentioned above, metal layer 102 grade which makes a counterelectrode of a stratified capacitor, Through these 1st and 2nd through hole conductors 107A and 107B, it was led to the surface and rear surfaces 110A and 110B of the core substrate 110, and has conducted with the metal layer 101,106, respectively.
[0058]In the state of this core substrate 110, existence and insulation resistance with a poor short circuit of the stratified capacitor C1, or electric capacity is checked. Thereby, when the metal layers 102 and 103 contact and short-circuit, for example and the stratified capacitor C1 is a short defect, in the case where electric capacity is outside a standard range, it is judged that the core substrate 110 is poor and it is discarded. Since noise rejection capability increases so that the electric capacity of a capacitor is large, it is preferred to make electric capacity high as much as possible, but for that purpose, it is thin in the thickness of complex-dielectrics layer 111 grade, Or in order to make the dielectric constant of a complex-dielectrics layer high for the area (specifically area of each metal layer) of the core substrate 110 further widely, the technique of making the addition of metal powder, such as copper powder, increase etc. can be considered.
[0059]However, since it is what carries out all of this technique that it is easy to produce the short defect of a capacitor, the short defect of a stratified capacitor increases and the yield falls easily. On the other hand, in this embodiment, since the check of a stratified capacitor is made in the state of the core substrate 110, Since a resin insulating layer etc. are not formed but a

fault article can be removed in the stage of the comparatively low core substrate 110 of added value, in the inside of the manufacturing process of the wiring board 100 which following-, or after manufacture, the fall of the yield by a poor stratified capacitor and the loss by an abandonment article can be suppressed low.

[0060]What is necessary is henceforth, just to form the wiring board 100 with a publicly known technique, using this core substrate 110 like the usual core substrate. As first shown in drawing 7, it is filled up with the plug material 116 which becomes the breakthrough 107H inside the through hole conductor 107 from an epoxy resin, and, specifically, the occlusion parts 101C and 106C are formed by plating.

[0061]Subsequently, after sticking a photosensitive epoxy resin film on the surface and rear surfaces 110A and 110B of the core substrate 110, carrying out exposure development and forming a via hole, make it harden, consider it as the resin insulating layer 121,131, and further with a semiadditive process. The wiring layer 125,135 which consists of copper and contains the beer conductors 125V and 135V is formed (refer to drawing 8).

[0062]After that, the wiring layer 145,155 which contains the resin insulating layer 141,151 and the beer conductors 145V and 155V similarly is formed, the resin insulating layer 161,171 which plays a role of a SOREDA resist is formed further, and the wiring board 100 is completed (refer to drawing 2).

[0063]So that he can understand easily from the above-mentioned explanation in this embodiment. Although the layered product 50 is formed, since the 3 layered film 10 and the patternizing 3 layered films 20 and 30 were used, There is no necessity of forming complex-dielectrics layer 111 grade and metal layer 101,102 grade in order, and since it prepares, and the 3 layered films 10 for a required number of layers and patternizing 3 layered-film 20 grade are laminated and can be formed at once, the core substrate 110 can be formed easily. Though this core substrate 110 is built [a stratified capacitor] in, since resin insulating layer 121 grade and wiring layer 125 grade can be formed in those surface and rear surfaces 110A and 110B by the same equipment and process as a case where the conventional core substrate is used, The wiring board 100 which built in a capacitor can form easily.

[0064](Modification) It ranks second and the core substrate 510 and the wiring board 500 of a modification of the above-mentioned Embodiment 1 are explained with reference to Drawings. The core substrate 510 and the wiring board 500 of this modification consist of the same construction material as the core substrate 110 of the above-mentioned Embodiment 1, and the wiring board 100, and have the almost same structure. However, although manufactured in the above-mentioned wiring board 100 in what is called stagger DOBIA form formed in the position which shifted the beer conductor 145 to the plane direction to the beer conductor 125V, it forms in this modification in the form of the stacked beer which accumulates a beer conductor on a thickness direction and forms it. Since it differs three sorts of through hole conductors 507A and 507B which the core substrate of this

modification forms, and in that arrangement of 507C has the feature, it explains focusing on a different portion, and it omits or simplifies and the same portion is explained.

[0065]First, the core substrate 510 concerning this modification is explained. As shown in the partial expanded sectional view of drawing 9, the core substrate 510, It laminates like the core substrate 110 of Embodiment 1 the five-layer complex-dielectrics layers 511-515, these complex-dielectrics layer 511 grade, and by turns, It has the metal layers 501-506 which consist of Cu formed in between the layer, the drawing 9 Nakashita side of the complex-dielectrics layer 511, and the drawing 9 Nakagami side of the complex-dielectrics layer 515, respectively, and the through hole conductor 507 which is formed in the inner skin of the breakthrough H and similarly consists of Cu(s). The complex-dielectrics layer 511 grade and the metal layer 501 grade which counters via these constitute the stratified capacitor C51 which has a dielectric layer of five layers. Direct continuation of the 1st inside metal layer 502,504 chosen every other layer among the inside metal layers 502-505 is carried out to the 1st through hole conductor 507A, and conduction is carried out to the metal layer 501,506 on the core substrate surface 110A or the rear face 110B of a core substrate, respectively. On the other hand, direct continuation of the 2nd inside metal layer 503,505 which was not chosen is carried out to the 2nd through hole conductor 507B, and conduction is carried out to the metal layer 501,506 in a similar manner. It is used as an electrode which constitutes the stratified capacitor C51, and also the outside metal layer 501,506 is used as a wiring layer.

[0066]Like the 3rd through hole conductor 507C, in order to use for signal wiring etc., there are some which are not conducted in the through hole conductor 507 with internal metal layer 502 grade. In this core substrate 510, as described above, a part of metal layers 502 and 504 and metal layers 501 and 506 have conducted mutually, and on the other hand, a part of metal layers 503 and 505 and metal layers 501 and 506 have conducted mutually. Therefore, these metal layers are making the stratified capacitor C51 by countering on both sides of each complex-dielectrics layer 511 grade. And three sorts of through hole conductors 507A, 507B, and 507C, Since it has extended to the surface 510A and the rear face 510B of the core substrate 510, the wiring layer formed in the rear-face 510B side of the core substrate 510 and the wiring layer formed in the surface 510A side are connectable via these through hole conductors 507. Here, since it means inserting the stratified capacitor C51 in parallel between power supply potential and earth potentials when the 1st through hole conductor 507A is connected to power supply wiring and the 2nd through hole conductor 507B is connected to grounding wiring, for example, the noise on which such potential is overlapped is absorbable. On the other hand, if it is connected with the 3rd through hole conductor 507C, signal wiring is in the state divorced from the stratified capacitor C51, and can let the inside of the core substrate 510 pass.

[0067]Subsequently, the wiring board 500 concerning this modification is

explained. The top view is shown in drawing 12, and the bottom view is shown for the partial expanded sectional view of the wiring board 500 in drawing 11 at drawing 13. The wiring board 500 has the almost same section structure as the above-mentioned Embodiment 1, The two-layer wiring layer 525,545,535,555 which consists of the resin insulating layers 521, 541, and 561,531,551,571 of three layers which consist of epoxy resins, respectively, and Cu is formed in the surface and rear surfaces 510A and 510B of the above-mentioned core substrate 510, respectively. It is formed between the layers of resin insulating layer 121 grade, and the beer conductors 525V, 545V, 535V, and 555V for connecting with the metal layer and wiring layer which are located in a lower layer are included in each wiring layer 525 grade. The inside of the through hole conductor 507 of the core substrate 510 is filled up with the plug material 516 which consists of epoxy resins, respectively, and it is closed by the occlusion parts 501C and 506C formed in the metal layer 501,506, respectively.

[0068]To the surface 500A side of this wiring board 500. As shown in a top view of drawing 12, many openings 561H formed in the resin insulating layer 561 are formed in the shape of an approximately lattice so that IC chip CH may be carried in a plane direction approximately center part and the terminal CHB of IC chip CH can be connected to a center section by flip chip bonding. In this opening 561H, the wiring layer 545 or the beer conductor 545V is exposed so that he can understand easily from drawing 11. On the other hand, as shown in a bottom view of drawing 13, the opening 571H was formed in the shape of a lattice all over almost [method / of the resin insulating layer 571 / of flat surface], and the wiring layer 555 containing the beer conductor 555V has exposed the rear-face 500B side of the wiring board 500 in the opening 571 for connection with other wiring boards, such as a mother board.

[0069]This wiring board 500 as well as the wiring board 100 of Embodiment 1 builds in the stratified capacitor C51 formed in the core substrate 510, and can connect IC chip CH and the stratified capacitor C51 which are carried in the wiring board surface 500A which is an IC chip mounting surface in a very near distance. Therefore, noise rejection can be performed certainly. Signal wiring can also be designed and taken about with the same line width as usual, and a design of a signal wiring layer wiring layer, etc. can be made easy. Since the occlusion parts 501C and 506C are formed and the beer conductors 525V and 535V are used as an occlusion part top beer conductor which carries out direct continuation of the occlusion part 501C etc., The through hole conductor 507 and occlusion part top beer conductor 525V grade can be connected in a very short distance, and resistance and an inductance which wiring layer 525 grade has can be reduced.

[0070]In this wiring board 500, there are some which are being made into stacked beer form of having accumulated the beer conductors 545V and 555V on the beer conductors 525V and 535V. A portion corresponding to an IC chip at the time of carrying IC chip CH in the wiring board 500 especially, at drawing 11, as a two-dot chain line shows, Namely, it forms in the above

stacked beer forms about wiring which ties the 1st and 2nd through hole conductors 507A and 507B in the IC corresponding point Q which projects IC chip CH on a thickness direction, and the terminal CHB of IC chip CH. Thus, since wiring between the stratified capacitor C51 and an IC chip can be especially shortened if form of stacked beer is used, it is useful to become low resistance and a low inductance further and to prevent invasion of a noise.
[0071]Since IC chip CH is carried in the wiring board surface 500A side here as mentioned above, and it connects with other wiring boards by the rear-face 500B side, within the wiring board 500, The wiring to which between the wiring layer 545 and the beer conductor 545V which are exposed in the opening 561H, and the wiring layers 555 exposed in the opening 571H is connected is formed. Therefore, as mentioned above to the core substrate 510, three sorts of through hole conductors 507 are formed, but in the core substrate 510 of this modification, as the through hole conductor 507 is shown in drawing 10, it arranges to a plane direction. In this figure, it is a black dot, and the 1st and 2nd through hole conductors 507A and 507B are expressed with a circle [white], and the 3rd through hole conductor 507 was easier to understand the difference in arrangement by the kind of through hole conductor, and is expressing them. The portion surrounded by the two-dot chain line even in this figure shows the IC corresponding point Q. this IC corresponding point Q -- the core substrate 510 -- it is mostly located in a center section. PP' section shown with a dashed line is equivalent to the section shown in drawing 9.
[0072]Within the IC corresponding point Q which is a center section, many 1st through hole conductors 507A and 2nd through hole conductors 507B are formed among three kinds of through hole conductors 507A, 507B, and 507C so that he can understand easily from drawing 10. On the other hand, a small number of formation is only carried out, and the 3rd through hole conductor 507C has become less than the number of the 1st and 2nd through hole conductors 507A and 507B. On the other hand, many 3rd through hole conductors 507C are formed in the peripheral edge part of the outside of the IC corresponding point Q, and if it sees about the 3rd through hole conductor 507C, the number formed in the peripheral edge part is increased rather than the number formed in the IC corresponding point Q. That is, many of 3rd through hole conductors 507C used for signal wiring etc. are formed in the peripheral edge part from the IC corresponding point Q.
[0073]Thus, it is from the following Reasons to arrange the through hole conductor 507. That is, it is preferred to follow the terminal CHB of IC chip CH with each electrodes (metal layer) 501-506 of the stratified capacitor C51 of the core substrate 510, and to connect the 1st through hole conductor 507A and the 2nd through hole conductor 507B in the shortest possible distance. For this reason, if it is desirable, and locating the 1st and 2nd through hole conductors 507A and 507B directly under IC chip CH forms many 1st and 2nd through hole conductors 507A and 507B and it moreover connects in parallel, The resistance of wiring which ties the 1st and 2nd through hole conductor

507A, etc. and these and an IC chip can be reduced further. Therefore, it is preferred to form many 1st and 2nd through hole conductors 507A and 507B in directly under [of IC chip CH / Q], i.e., IC corresponding point. On the other hand, since signal wiring using the 3rd through hole conductor 507C cannot ask for their being low resistance and a low inductance so much, if it says from the field of resistance or an inductance, it is not necessary to necessarily form it in the IC corresponding point Q. Therefore, by arranging the 3rd through hole conductor 507C to the peripheral edge part of the IC corresponding point Q as much as possible, the necessity of taking into consideration the 3rd through hole conductor 507C decreases, and many 1st and 2nd through hole conductors 507A etc. can be easily arranged now. That is, the stratified capacitor C51 and IC chip CH can be connected more now with low resistance and a low inductance.

[0074]It not only formed the beer conductors 525V and 535V in the occlusion parts 501C and 506C provided in the through hole conductor 507 in piles directly, but in the wiring board 500 of this modification, it forms wiring in the stacked beer form of having accumulated the beer conductor 525V, and 545V, 535V and 555V. For this reason, it is further connectable with IC chip CH at low resistance and a low inductance. In this wiring board and core substrate 510. In consideration of arrangement of three sorts of through hole conductors 507, in the IC corresponding point Q of a center section. Arrange so that the 1st and 2nd through hole conductors 507A and 507B may increase more than the 3rd through hole conductor 507C, and moreover, the 3rd through hole conductor 507C, Since it was made for the number with which the peripheral edge part of the IC corresponding point Q was formed to increase more than the number of what was formed in the IC corresponding point Q, Many 1st and 2nd through hole conductors 507A and 507B can be formed easily, and the stratified capacitor 51 and IC chip CH can be further connected with low resistance and a low inductance. Formation of the core substrate 510 and the wiring board 500 of this modification is good like the above-mentioned Embodiment 1.

[0075](Embodiment 2), next a 2nd embodiment are described. Since it differs from Embodiment 1 at the point which has the central substrate 211 at the center, and equipped the surface and rear surface with the stratified capacitor, the core substrate 210 of this embodiment is explained focusing on a different portion, and it omits or simplifies and it explains the same portion.

[0076]The core substrate 210 of this embodiment shown in drawing 14 is provided with the following.

The central substrate 211 with a thickness of 600 micrometers which consists of a glass fiber-epoxy resin composite material.

The stratified capacitor C21, C22 which were formed in the surface and rear surfaces 211A and 211B, respectively.

concrete -- the central substrate 211 and 50 micrometers in thickness -- $BaTiO_3$ powder -- 30vol% and Cu powder -- 20vol% -- with the complex-dielectrics layer 212,213 which consists of a ceramic metal-resin composite material distributed

in the epoxy resin. It has the metal layers 201,203 and 202,204 which counter on both sides of this, respectively, and consist of Cu(s), and also has the through hole conductor 207 which is further formed in the inner skin of the breakthrough H, and similarly consists of Cu(s). The complex-dielectrics layer 212,213, the metal layer 201 which counters via these, and 203, 202 and 204 constitute the respectively stratified capacitor C21 and C22. Conduction of the metal layer 201,202 of an internal layer is carried out to the metal layer 203,204 on the core substrate surface 210A or the rear face 210B of a core substrate by the 1st through hole conductor 207A or the 2nd through hole conductor 207B, respectively.

[0077]That is, the inside of the metal layer by which the 1st through hole conductor 207A is contained in the stratified capacitor C21 by the side of the surface, Direct continuation is carried out to the metal layer 203 which makes one electrode of this stratified capacitor C21, and direct continuation is carried out to the metal layer 202 which makes one electrode of this stratified capacitor C22 further among the metal layers contained in the stratified capacitor C22 by the side of a rear face.The inside of the metal layer by which the 2nd through hole conductor 207B is contained in the stratified capacitor C21 by the side of the surface, Direct continuation is carried out to the metal layer 201 which makes the electrode of another side of this stratified capacitor C21, and direct continuation is carried out to the metal layer 204 which makes the electrode of another side of this stratified capacitor C22 further among the metal layers contained in the stratified capacitor C22 by the side of a rear face.

[0078]It is used also as the stratified capacitor C21 and an electrode which constitutes C22, and also the outside metal layer 203,204 is used as a wiring layer. Like the 3rd through hole conductor 207C, in order to use for signal wiring etc., there are some which are not conducted in the internal metal layer 201,202 in the through hole conductor 207. And three sorts of through hole conductors 207A, 207B, and 207C, Since it has extended to the surface 210A and the rear face 210B of the core substrate 210, the wiring layer formed in the rear-face 210B side of the core substrate 210 and the wiring layer formed in the surface 210A side are connectable via these through hole conductors 207.

[0079]This core substrate 210 forms the one-layer complex-dielectrics layer 212,123 and the two-layer metal layers 201,203 and 202,204 in that surface 211A and rear face 211B centering on the central substrate 211, respectively. And if the surface sees about a layer corresponding to peace and the back side, such construction material is same material and is made into the same thickness. Therefore, curvature by such imbalance does not generate this core substrate 201 easily.

[0080]Since the stratified capacitor C21 and C22 are built in, also in this core substrate 210, like the core substrate 110 of Embodiment 1, so that he can understand easily, When a resin insulating layer and a wiring layer are further formed in this core substrate 210 and a wiring board is manufactured, since [of an IC chip] a capacitor will be arranged very much to the

neighborhood, invasion of a noise can be prevented effectively. If connecting the 1st through hole conductor 207A to power supply wiring and connecting the 2nd through hole conductor 207B to grounding wiring, for example, speaking concretely, Since it means inserting the stratified capacitor C21 and 22 in parallel between power supply potential and earth potentials, a noise on which such potential is overlapped is absorbable. If it is connected with the 3rd through hole conductor 207C, signal wiring is in the stratified capacitor C21 and a state divorced from 22, and can let inside of the core substrate 210 pass.
[0081]In this core substrate 210, it is thicker than the complex-dielectrics layer 212,213, Since the metal layer 201 grade and the complex-dielectrics layer 212,213 are formed in these surface and rear surfaces 211A and 211B using the central substrate 211 which consists of a glass fiber-epoxy resin composite material, The mechanical strength of the core substrate 210 is high, and since it can be equal to modification etc., handling becomes still easier. Since the rigidity of the central substrate 211 is high, it is because this can be made to support the rigidity of the core substrate 210 whole. In the above-mentioned Embodiment 1, the complex-dielectrics layers 111-115 which all mixed BaTiO3 powder and Cu powder in the epoxy resin were used as a dielectric layer of the stratified capacitor C1. However, although electric capacity falls, a part of dielectric layer which constitutes a stratified capacitor, such as replacing with the complex-dielectrics layer 111,115 and, using the dielectric layer by the resin which is not mixing BaTiO3 powder and also Cu powder for example, may be the construction material which does not contain high dielectric powder.
[0082]Subsequently, the wiring board 200 is explained. The wiring board 200 shown in drawing 15 to the surface and rear surfaces 210A and 210B of the above-mentioned core substrate 210. The two-layer wiring layer 225,245,235,255 which consists of the resin insulating layers 221, 241, and 261,231,251,271 of three layers which consist of epoxy resins, and Cu like Embodiment 1 is formed, respectively. Each wiring layer 225 grade is formed between the layers of resin insulating layer 221 grade, and it contains the beer conductors 225V, 245V, 235V, and 255V. The inside of the through hole conductor 207 of the core substrate 210 is filled up with the plug material 216 which consists of epoxy resins, respectively, and it is closed by the occlusion parts 203C and 204C formed in the metal layer 203,204, respectively.
[0083]A stratified capacitor formed in the core substrate 210 is built in, an IC chip (not shown) and a stratified capacitor which are carried in the wiring board surface 100A can be connected in a very near distance, and this wiring board 200 can also perform noise rejection certainly. Wiring layer 225 grade can be designed and taken about with the same line width as usual like Embodiment 1. Therefore, a design of a signal wiring layer wiring layer, etc. can be made easy.
[0084]The occlusion parts 203C and 204C are formed, and the beer conductors 225V and 235V are formed on this occlusion part 203C and 204C, respectively. These beer conductors 225V and 235V are the occlusion parts 203C and 204C

and an occlusion part top beer conductor which carries out direct continuation. Since the through hole conductor 107 and the beer conductors 225V and 235V are connectable in a very short distance if it does in this way, resistance and an inductance which wiring layer 225 grade has can be reduced. Therefore, especially, wiring between the stratified capacitor C21, and C22 and an IC chip is shortened, and it is useful to prevent invasion of a noise as low resistance and a low inductance. in addition -- manufacturing in the form of stagger DOBIA formed in Embodiment 1 while shifting a position of each beer conductor 125 grade -- (refer to drawing 2) -- in this wiring board 200, Each beer conductor 225V, and 245V, 235V and 255V are formed in the form of a heap of states, i.e., stacked beer, so that he can understand easily from drawing 15. If it forms from this stacked beer, the length of wiring which pulls out to the wiring board surface 200A, an electrode, i.e., metal layer 201 grade, of a capacitor, will be made short, And since the beer conductors 225V and 235V which are located downward unlike dished stagger DOBIA serve as form with which a conductor was filled up, wiring can also be formed thickly and resistance becomes low. Therefore, since an inductance which wiring has becomes small, invasion of a noise can be controlled further.

[0085]Subsequently, a manufacturing method of the above-mentioned core substrate 210 is explained. A three-layer film formation process is the same (refer to drawing 3) with Embodiment 1. On the other hand, as shown in drawing 16, the metal layer 201,202 of a prescribed pattern is beforehand formed in the surface and rear surfaces 211A and 211B of the central substrate 211, respectively.

[0086]Then, in a laminate sheet formation process, as shown in drawing 17 (a), as the metal layer 201,202 and the semi-hardening complex-dielectrics layer 12 lap, they laminate the double film 10C which removed reinforcement film RF of the 3 layered film 10, respectively. Then, in a vacuum, heat pressing is carried out to figure Nakagami down on condition of 180 x2Hr and 30kg[/cm] ^{2}, an epoxy resin of a complex-dielectrics layer is stiffened, and the layered product 60 shown in drawing 17 (b) is formed at once. As for this layered product 60, the metal layer 201,202 of a prescribed pattern, the complex-dielectrics layer 212,213, and the copper foil 11 and 11 are laminated by the surface and rear surfaces 211A and 211B of the central substrate 211, respectively.

[0087]Then, in a through-hole formation process, as shown in drawing 18, the surface and rear surface 60A of this laminate sheet 60 and the breakthrough H with a diameter of 60 micrometers which penetrates between 60B are punched in a specified position using the 4th harmonics of an YAG laser. What the end faces 201H and 202H of the metal layer 201,202 expose is formed in the inner skin of the punched breakthrough H. That is, the 1st breakthrough H4 that the metal layer 202 exposes to inner circumference, the 2nd breakthrough H5 that the metal layer 201 exposes to inner circumference, and the 3rd breakthrough H6 that exposes neither of the metal layer 201,202 are formed.

[0088]In a surface and rear surface metal layer formation process, form the

through hole conductor 207 with the publicly known PTH formation technique in the breakthrough H, and. Using the copper foil 11 and 11 of the laminate sheet surface and rear surfaces 60A and 60B, the metal layer 203,204 of a prescribed pattern is formed and the core substrate 210 is completed (refer to drawing 14). The metal layer 201,202 among [207A and 207B] the through hole conductors 207 (for example, the 1st and 2nd through hole conductors), Since it conducts in the end-face 201H grade, respectively, as mentioned above, the metal layer 201,202 which makes the counterelectrode of a stratified capacitor, Through these 1st and 2nd through hole conductors 207A and 207B, it was led to the surface and rear surfaces 210A and 210B of the core substrate 210, and has conducted with the metal layer 203,204, respectively.

[0089]Thus, if the core substrate 210 is completed, the stratified capacitor C21, existence and insulation resistance with a poor short circuit of C22, or electric capacity will be checked in the state of this core substrate 210 like Embodiment 1. If the short defect of a stratified capacitor, electric capacity substandard, etc. are detected by this when the metal layers 201 and 203 contact and short-circuit, for example, the poor core substrate 210 will be discarded. Also in this core substrate 210, since it is preferred like the above-mentioned core substrate 110 to make electric capacity high, it can consider making thin thickness of complex-dielectrics layer 212 grade, and making area of the core substrate 210 large, or making the metal-powder addition of a complex-dielectrics layer increase. However, by these, the short defect of a stratified capacitor increases and the yield falls easily. On the other hand, in the core substrate 210, since the quality check of a stratified capacitor is made in this state, Since a fault article is removable in the stage of the comparatively low core substrate 210 of added value, the fall of the yield by the poor stratified capacitor in the manufacturing process of the wiring board 200 which following-, or after manufacture, and the loss by an abandonment article can be suppressed low.

[0090]What is necessary is henceforth, just to form the wiring board 200 with a publicly known technique like Embodiment 1, using this core substrate 210 like the usual core substrate. As shown in drawing 19, it is filled up with the plug material 216 which becomes a breakthrough inside the through hole conductor 207 from an epoxy resin, and, specifically, the occlusion parts 203C and 204C are formed by plating. Subsequently, as shown in drawing 20, a photosensitive epoxy resin film is stuck on the surface and rear surfaces 210A and 210B of the core substrate 210, After carrying out exposure development and forming a via hole, it is made to harden, and it is considered as the resin insulating layer 221,231, and the wiring layer 225,235 which contains further the beer conductors 225V and 235V which consist of copper with a semiadditive process is formed. After that, the wiring layer 245,255 which contains the resin insulating layer 241,251 and the beer conductors 245V and 255V like the above is formed, the resin insulating layer 261,271 which plays the role of a SOREDA resist is formed further, and the wiring board 200 is completed (refer to drawing 15).

[0091]Although the above-mentioned embodiment showed the example in which the stratified capacitor C22 which becomes the rear face 211B from the metal layer 202,204 and the complex-dielectrics layer 213 again about the stratified capacitor C21 which consists of the metal layer 201,203 and the complex-dielectrics layer 212 was formed on the surface 211A of the central substrate 211, When the electric capacity to need is small, a stratified capacitor may be formed in either the surface or a rear face according to a case.

[0092]Or when the electric capacity to need is large contrary to this, The stratified capacitor C41 and the complex-dielectrics layer of C42 which are formed in the surface and rear surface of the central substrate 211 are made into plurality (at drawing 21, it is two-layer [212,414 and 213,415], respectively), respectively like the core substrate 410 shown in drawing 21 as a modification of Embodiment 2, A metal layer (drawing 21 metal layers 201, 403, and 405,202,404,406) is formed these and by turns, request metal layers are mutually connected by the through hole conductor 407, and it may be made to secure the electric capacity of a capacitor.

[0093]In this core substrate 410, the 1st through hole conductor 407A, Direct continuation is carried out to the metal layer 403 which makes one electrode of this stratified capacitor C41 among metal layers contained in the stratified capacitor C41 by the side of the surface, Direct continuation is carried out to the metal layer 202,406 which makes one electrode of this stratified capacitor C42 among metal layers contained in the stratified capacitor C42 by the side of a rear face. Inside of a metal layer by which the 2nd through hole conductor 407B is contained in the stratified capacitor C41 by the side of the surface, Direct continuation is carried out to the metal layer 201,405 which makes an electrode of another side of this stratified capacitor C41, and direct continuation is carried out to the metal layer 404 which makes an electrode of another side of this stratified capacitor C42 further among metal layers contained in the stratified capacitor C42 by the side of a rear face. As for the 3rd through hole conductor 407C of non-conduction, any of an electrode of the stratified capacitor 41 by the side of the surface and the stratified capacitor 42 by the side of a rear face are contained.

[0094]As a manufacturing method of this core substrate 410, the patternizing copper foil 21 of a desired pattern besides the 3 layered film 10 and the patternizing 3 layered films 20 and 30 (refer to drawing 4) in which 31 grades were formed are prepared beforehand. And on the metal layer 201,202 beforehand formed in the surface and rear surfaces 211A and 211B of the central substrate 211, What is necessary is to laminate previously patternizing 3 layered-film 20 grade which removed reinforcement film RF, respectively, to laminate and carry out heat pressing of the 3 layered films 10 which removed reinforcement film RF after that, to form a layered product, and just to form like the above after that.

[0095]Also in this embodiment or its modification, there is no necessity of forming the complex-dielectrics layer 212,213 and metal layer 201,202 grade

in order although layered product 60 grade is formed so that he can understand easily from the above-mentioned explanation. That is, patternizing 3 layered-film 20 grade is prepared further, and the central substrate 211 in which the metal layer 201,202 was formed, the 3 layered films 10, and since it laminates these and can form at once, the core substrate 210,410 can be formed easily. The core substrate 210,410 which was carried out in this way and formed, Though a stratified capacitor is built in, since resin insulating layer 221 grade and wiring layer 225 grade can be formed in the surface and rear surfaces 210A, 210B, and 410A by the same equipment and process as the case where the conventional core substrate is used, the wiring board 200 etc. which built in the capacitor can form easily.

[0096]Although it was based on Embodiments 1 and 2 and the modification of those and this invention was explained above, this invention is a range which is not limited to the above-mentioned embodiment etc. and does not deviate from the summary, and it cannot be overemphasized that it changes suitably and can apply. For example, although Embodiment 1 showed the core substrate 110 which laminated a five-layer complex-dielectrics layer, it can change suitably, such as increasing or reducing a number of layers according to required electric capacity. Although the thing which made the epoxy resin distribute $BaTio_3$ powder and Cu powder was used as a complex-dielectrics layer, other high permittivity powder metallurgy group powder can also be used. The 3 layered films 10 which all removed reinforcement film RF in the above-mentioned embodiment, the patternizing 3 layered films 30 [20 and] 10C, i.e., a bilayer film, or the patternizing bilayer films 20C and 30C, It laminated in piles directly in the copper foil 11 and 41, the patternizing copper foil 21, and 31 grades. However, arrange spreading or a binder film for the adhesives which consist of epoxy resins etc., an adhesives layer is made to intervene, and it laminates, and heat pressing may be carried out and a layered product may be formed. In this case, it can be considered as the layered product on which the complex-dielectrics layer 111 grade and the metal layer 102 grade were pasted up certainly.

[0097]Although the 3 layered films 10 and the patternizing 3 layered films 20 and 30 which stuck reinforcement film RF were used in the above-mentioned embodiment, After taking handling and others into consideration, it may be made to use only the bilayer film 10C and the patternizing bilayer films 20C and 30C, without using reinforcement film RF.

[Brief Description of the Drawings]

[Drawing 1]It is a partial expanded sectional view of the core substrate concerning Embodiment 1.

[Drawing 2]It is a partial expanded sectional view of the wiring board concerning Embodiment 1.

[Drawing 3]The state in which (a) formed the complex-dielectrics layer on copper foil, and the state where (b) stuck the reinforcement film and 3 layered films were formed are shown among the manufacturing methods of the core substrate and wiring board concerning Embodiment 1.

[Drawing 4]The state in which (a) formed the etching resist of the prescribed pattern on copper foil, the state which (b) etched copper foil and was fabricated to the prescribed pattern, and the state where (c) molded copper foil into the pattern different from (b) are shown among the manufacturing methods of the core substrate and wiring board concerning Embodiment 1.
[Drawing 5](a) shows the laminate sheet fabricated by (b's) laminating signs that a reinforcement film is removed and laminated, and pressing from 3 layered films among the manufacturing methods of the core substrate and wiring board concerning Embodiment 1.
[Drawing 6]The state where the breakthrough was formed is shown in the laminate sheet shown in drawing 5 among the manufacturing methods of the core substrate and wiring board concerning Embodiment 1.
[Drawing 7]It is a partial expanded sectional view showing the state where the bore which was filled up with resin in the bore of the center of a through hole conductor of the core substrate shown in drawing 1 among the manufacturing methods of the wiring board concerning Embodiment 1, and formed the conductor also in the upper and lower sides of a bore was closed.
[Drawing 8]It is a partial expanded sectional view showing the state where the resin insulating layer and the wiring layer were formed on the surface and rear surface of the core substrate shown in drawing 7 among the manufacturing methods of the wiring board concerning Embodiment 1.
[Drawing 9]It is a partial expanded sectional view of the core substrate concerning the modification of Embodiment 1.
[Drawing 10]It is a figure showing arrangement of the through hole conductor of the core substrate concerning the modification of Embodiment 1.
[Drawing 11]It is a partial expanded sectional view of the wiring board concerning the modification of Embodiment 1.
[Drawing 12]It is a top view of the wiring board concerning the modification of Embodiment 1.
[Drawing 13]It is a bottom view of the wiring board concerning the modification of Embodiment 1.
[Drawing 14]It is a partial expanded sectional view of the core substrate concerning Embodiment 2.
[Drawing 15]It is a partial expanded sectional view of the wiring board concerning Embodiment 2.
[Drawing 16]It is a partial expanded sectional view of the central substrate which equips a surface and rear surface with the metal layer of a prescribed pattern among the manufacturing methods of the core substrate and wiring board concerning Embodiment 2.
[Drawing 17](a) shows the surface and rear surface laminate sheet fabricated by (b's) laminating signs that 3 layered films which removed the reinforcement film, respectively to the surface and rear surface of the central substrate shown in drawing 11 are laminated, and pressing among the manufacturing methods of the core substrate and wiring board concerning Embodiment 2.
[Drawing 18]The state where the breakthrough was formed is shown in the

surface and rear surface laminate sheet shown in drawing 12 among the manufacturing methods of the core substrate and wiring board concerning Embodiment 2.
[Drawing 19]It is a partial expanded sectional view showing the state where the bore which was filled up with resin in the bore of the center of a through hole conductor of the core substrate shown in drawing 9 among the manufacturing methods of the wiring board concerning Embodiment 2, and formed the conductor also in the upper and lower sides of a bore was closed.
[Drawing 20]It is a partial expanded sectional view showing the state where the resin insulating layer and the wiring layer were formed on the surface and rear surface of the core substrate shown in drawing 14 among the manufacturing methods of the wiring board concerning Embodiment 2.
[Drawing 21]It is a partial expanded sectional view showing the modification of the core substrate concerning Embodiment 2.
[Drawing 22]It is a partial expanded sectional view showing the conventional wiring board which carries a chip capacitor in the undersurface.
[Explanations of letters or numerals]
110,210,410,510 core substrates
110A, 210A, 410A, the 510A core substrate surface
110B, 210B, 410B, a 510B core substrate rear face
100,200,500 Wiring board
111, 112, 113, 114, 115, 212, 213, 414, 415, 511, and 512,513,514,515 Complex-dielectrics layer
101,102,103, 104,105,106, 201,202,203, 204,403,404, 405,406,501, 502, and 503,504,505,506 Metal layer
107,207,407,507 Through hole conductor
107A, 207A, and 507A The 1st through hole conductor
107B, 207B, and 507B The 2nd through hole conductor
107C, 207C, and 507C The 3rd through hole conductor
C1, C21, C22, C41, C42, and C51 Stratified capacitor
121, 131, 141, 151, 161, 171, 221, 231, 241, 251, 261, 271, 521, and 531,541,551,561 Resin insulating layer
125, 135, 145, 155, 225, 235, 245, 255, and 525,535,545,555 Wiring layer
125V, 135V, 145V, 155V, 225V, 235V, 245V, 255V, 525V, 535V, 545V, and 555V Beer conductor
211 A central substrate
211A A central substrate face
211B A central substrate rear
10 3 layered films
11 and 41 Copper foil
12 Semi-hardening complex-dielectrics layer
21, 31 patternizing copper foil
RF Reinforcement film
50 and 60 Layered product

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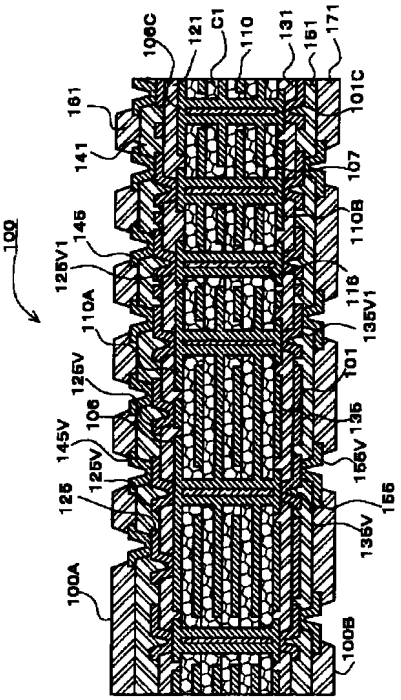
(54)【発明の名称】　配線基板、コア基板及びその製造方法

(57)【要約】
【課題】　搭載するＩＣチップの近くにコンデンサを内蔵し、しかも製造容易で、歩留まりが高く、製造工程中にコンデンサの不具合が発見されても損失金額が少ない構造とした配線基板、およびそのような配線基板に用いるコア基板、さらには、このコア基板の容易かつ安価な製造方法を提供する。
【解決手段】　配線基板１００は、コア基板１１０とこのコア基板１１０の表面１１０Ａおよび裏面１１０Ｂにそれぞれ積層された３層の樹脂絶縁層１２１～１７１と、この樹脂絶縁層同士の間に配線層１２５～１５５とを有する。コア基板１１０は、エポキシ樹脂及びＢａＴｉＯ３粉末を含む複合誘電体層１１１～１１５とこれを挟んで対向する複数の金属層１０１～１０６とから構成される層状コンデンサＣ１を備え、内層金属層１０２～１０５は、第１，第２スルーホール導体１０７Ａ，１０７Ｂで１層おきに接続されている。



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【特許請求の範囲】

【請求項１】コア基板と、上記コア基板の表面及び裏面に積層された１または複数の樹脂絶縁層と、上記コア基板の表面側及び裏面側において、上記コア基板と上記樹脂絶縁層の間及び上記樹脂絶縁層同士の間の少なくともいずれかに形成された配線層と、を有する配線基板であって、

上記コア基板は、

樹脂および高誘電体粉末を含む複数の複合誘電体層と、

上記複数の複合誘電体層と交互に積層され、これらの層間及び最下層の上記複合誘電体層の下面及び最上層の上記複合誘電体層の上面に形成され、上記複合誘電体層を挟んで対向する複数の金属層と、

上記複数の複合誘電体層及び複数の金属層を貫通する貫通孔内に形成され、上記コア基板表面及びコア基板裏面まで延びる複数のスルーホール導体と、

を備え、

上記複数の複合誘電体層と上記複数の金属層とは、層状コンデンサを構成し、

上記複数のスルーホール導体は、

上記複数の金属層のうち上記層間に形成された内側金属層から１層おきに選択した第１内側金属層に直接接続する複数の第１スルーホール導体と、

上記内側金属層のうち上記第１スルーホール導体とは非接続の第２内側金属層と直接接続する複数の第２スルーホール導体と、

上記内側金属層のいずれとも非導通の複数の第３スルーホール導体と、

を含む、配線基板。

【請求項２】コア基板と、上記コア基板の表面および裏面に積層された１または複数の樹脂絶縁層と、上記コア基板の表面側及び裏面側において、上記コア基板と上記樹脂絶縁層の間及び上記樹脂絶縁層同士の間の少なくともいずれかに形成された配線層とを有する配線基板であって、

上記コア基板は、

中心基板と、

この中心基板の表面および裏面にそれぞれ形成され、樹脂および高誘電体粉末を含む１または複数の複合誘電体層とこれを挟んで対向する複数の金属層とを交互に積層してなる層状コンデンサと、

上記表面側の層状コンデンサ、上記中心基板、上記裏面側の層状コンデンサを貫通する貫通孔内に形成され、上記コア基板表面及びコア基板裏面まで延びる複数のスルーホール導体と、

を備え、

上記複数のスルーホール導体は、

上記表面側の層状コンデンサに含まれる上記複数の金属層のうち、表面側層状コンデンサの一方の電極をなす１または複数の金属層に直接接続し、上記裏面側の層状コンデンサに含まれる上記複数の金属層のうち、裏面側層状コンデンサの一方の電極をなす１または複数の金属層に直接接続する第１スルーホール導体と、

上記表面側の層状コンデンサに含まれる上記複数の金属層のうち、表面側層状コンデンサの他方の電極をなす１または複数の金属層に直接接続し、上記裏面側の層状コンデンサに含まれる上記複数の金属層のうち、裏面側層状コンデンサの他方の電極をなす１または複数の金属層に直接接続する第２スルーホール導体と、

上記表面側層状コンデンサ及び裏面側層状コンデンサの電極のいずれとも非導通の第３スルーホール導体と、を含む配線基板。

【請求項３】請求項１または請求項２に記載の配線基板であって、

前記コア基板のうち、

上記配線基板の表面に搭載されるＩＣチップの搭載位置を厚さ方向に投影してなるＩＣ対応部には、前記３種のスルーホール導体のうち、前記第１スルーホール導体及び第２スルーホール導体が形成され、前記第３スルーホール導体は形成されないか、またはこのＩＣ対応部に形成された前記第１スルーホール導体と第２スルーホール導体の和よりも少数形成され、

上記ＩＣ対応部の周縁部には、上記第３スルーホール導体が上記ＩＣ対応部よりも多く形成されている配線基板。

【請求項４】その表面及び裏面に１または複数の樹脂絶縁層及び配線層を形成して配線基板とするためのコア基板であって、

樹脂および高誘電体粉末を含む複数の複合誘電体層と、

上記複数の複合誘電体層と交互に積層され、これらの層間及び最下層の上記複合誘電体層の下面及び最上層の上記複合誘電体層の上面に形成され、上記複合誘電体層をそれぞれ挟んで対向する複数の金属層と、

上記複数の複合誘電体層及び複数の金属層を貫通する貫通孔内に形成され、上記コア基板表面及びコア基板裏面まで延びる複数のスルーホール導体と、を備え、

上記複数の複合誘電体層と上記複数の金属層とは、層状コンデンサを構成し、

上記複数のスルーホール導体は、

上記複数の金属層のうち上記層間に形成された内側金属層から１層おきに選択した第１内側金属層に直接接続する第１スルーホール導体と、

上記内側金属層のうち上記第１スルーホール導体とは非接続の第２内側金属層と直接接続する第２スルーホール導体と、

上記内側金属層のいずれとも非導通の第３スルーホール導体と、

を含む、コア基板。

【請求項５】その表面及び裏面に１または複数の樹脂絶縁層及び配線層を形成して配線基板とするためのコア基

板であって、
中心基板と、
この中心基板の表面および裏面にそれぞれ形成され、樹脂および高誘電体粉末を含む１または複数の複合誘電体層とこれを挟んで対向する複数の金属層とを交互に積層してなる層状コンデンサと、
上記表面側の層状コンデンサ、上記中心基板、上記裏面側の層状コンデンサを貫通する貫通孔内に形成され、上記コア基板表面及びコア基板裏面まで延びる複数のスルーホール導体と、を備え、
上記複数のスルーホール導体は、
上記表面側の層状コンデンサに含まれる上記複数の金属層のうち、表面側層状コンデンサの一方の電極をなす１または複数の金属層に直接接続し、上記裏面側の層状コンデンサに含まれる上記複数の金属層のうち、裏面側層状コンデンサの一方の電極をなす１または複数の金属層に直接接続する第１スルーホール導体と、
上記表面側の層状コンデンサに含まれる上記複数の金属層のうち、表面側層状コンデンサの他方の電極をなす１または複数の金属層に直接接続し、上記裏面側の層状コンデンサに含まれる上記複数の金属層のうち、裏面側層状コンデンサの他方の電極をなす１または複数の金属層に直接接続する第２スルーホール導体と、
上記表面側層状コンデンサ及び裏面側層状コンデンサの電極のいずれとも非導通の第３スルーホール導体と、
を含む、コア基板。
【請求項６】請求項４または請求項５に記載のコア基板であって、
コア基板の平面方向中央部には、前記３種のスルーホール導体のうち、前記第１スルーホール導体及び第２スルーホール導体が形成され、前記第３スルーホール導体は形成されないか、この中央部に形成された前記第１スルーホール導体と第２スルーホール導体との和よりも少数形成されており、
コア基板の平面方向周縁部には、上記第３スルーホール導体が上記中央部よりも多数形成されているコア基板。
【請求項７】層状コンデンサを構成する、樹脂および高誘電体粉末を含む複数の複合誘電体層と、上記複合誘電体層をそれぞれ挟んで対向する複数の金属層と、を備えるコア基板の製造方法であって、
金属箔と、半硬化の樹脂と高誘電体粉末とを含む半硬化複合誘電体層と、補強フィルムとをこの順に有する三層フィルムを形成する三層フィルム形成工程と、
上記三層フィルムの金属箔を所定パターンに成形し、パターン化金属箔と半硬化複合誘電体層と補強フィルムとからなるパターン化三層フィルムを形成するパターン化三層フィルム形成工程と、
上記補強フィルムが剥がされた１の上記三層フィルムと１または複数の上記パターン化三層フィルムとを、上記１の三層フィルムの金属箔を最下層として半硬化複合誘電体層とパターン化金属箔とが交互に重なるように積層し、最上面の上記半硬化複合誘電体層に金属箔を重ね、熱プレスして、積層板を形成する積層板形成工程と、
上記積層板の表裏面を貫通する複数の貫通孔を形成する貫通孔形成工程と、
上記貫通孔内にスルーホール導体を形成すると共に、上記積層体の表裏面に表面側金属層及び裏面側金属層を形成する表裏面金属層形成工程と、を備えることを特徴とするコア基板の製造方法。
【請求項８】請求項７に記載のコア基板の製造方法であって、
前記貫通孔形成工程は、
前記パターン化金属箔から１層おきに選択した第１パターン化金属箔が内周に露出する第１貫通孔と、
上記パターン化金属箔のうち上記第１パターン化金属箔に選択されなかった残余の第２パターン化金属箔が内周に露出する第２貫通孔と、
上記パターン化金属箔のいずれも内周に露出しない第３貫通孔と、
を形成するコア基板の製造方法。
【請求項９】中心基板と、この中心基板の表面及び裏面のうち少なくともいずれかに、層状コンデンサを構成する、樹脂および高誘電体粉末を含む複合誘電体層と、これを挟んで対向する複数の金属層と、を備えるコア基板の製造方法であって、
金属箔と、半硬化の樹脂と高誘電体粉末とを含む半硬化複合誘電体層と、補強フィルムとをこの順に有する三層フィルムを形成する三層フィルム形成工程と、
表面及び裏面のうち少なくともいずれかに所定パターンの金属層を備える中心基板の上記金属層に、上記補強フィルムが剥された上記三層フィルムの半硬化複合誘電体層を重ね、熱プレスして、積層板を形成する積層板形成工程と、
上記積層板の表裏面を貫通する複数の貫通孔を形成する貫通孔形成工程と、
上記貫通孔内にスルーホール導体を形成すると共に、上記積層板の表裏面に表面側金属層及び裏面側金属層を形成する表裏面金属層形成工程と、を備えることを特徴とするコア基板の製造方法。
【請求項１０】中心基板と、この中心基板の表面及び裏面のうち少なくともいずれかに、層状コンデンサを構成する、樹脂および高誘電体粉末を含む複数の複合誘電体層と、上記複合誘電体層をそれぞれ挟んで対向する複数の金属層と、を備えるコア基板の製造方法であって、
金属箔と、半硬化の樹脂と高誘電体粉末とを含む半硬化複合誘電体層と、補強フィルムとをこの順に有する三層フィルムを形成する三層フィルム形成工程と、
上記三層フィルムの金属箔を所定パターンに成形し、パターン化金属箔と半硬化複合誘電体層と補強フィルムとからなるパターン化三層フィルムを形成するパターン化

三層フィルム形成工程と、
表面及び裏面のうち少なくともいずれかに所定パターンの金属層を備える中心基板の上記金属層上に、上記補強フィルムが剥がされた１または複数の上記パターン化三層フィルムを、上記金属層またはパターン化金属箔と半硬化複合誘電体層とが重なるように積層し、最上面の上記パターン化金属箔上に上記補強フィルムが剥がされた１の上記三層フィルムの半硬化複合誘電体層が重なるように積層し、熱プレスして、積層板を形成する積層板形成工程と、
上記積層板の表裏面を貫通する複数の貫通孔を形成する貫通孔形成工程と、
上記貫通孔内にスルーホール導体を形成すると共に、上記積層板の表裏面に表面側金属層及び裏面側金属層を形成する表裏面金属層形成工程と、を備えることを特徴とするコア基板の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、コア基板とこの表裏面に積層された樹脂絶縁層と配線層とを有する配線基板、コア基板及びコア基板の製造方法に関し、特に、コンデンサを内蔵し、ノイズの侵入を防止した配線基板、コア基板及びその製造方法に関する。

【０００２】

【従来の技術】従来より、ＩＣチップのアース配線と電源配線との間にノイズ除去用のデカップリングコンデンサを設けることが行われており、例えば、配線基板の表面や裏面等にチップコンデンサを搭載したものが用いられている。図２２に示す配線基板３００では、コア基板３１０の表裏面（図中上下面）にそれぞれ３層の樹脂絶縁層３２０，３４０，３６０，３３０，３５０，３７０が積層形成され、各層間には、配線層３１５，３２５，３４５，３３５，３５５が形成されている。さらに、この配線基板３００の基板裏面（図中下面）３００Ｂには、チップキャパシタＣＣがハンダＳＬによって配線層（パッド）３５５に搭載されている。この配線基板３００では、チップキャパシタＣＣの２つの電極ＣＣＡ，ＣＣＢは、各配線層３２５等およびスルーホール導体３１６を通じて、配線基板３００の基板上面３００Ａ、即ち、配線層（パッド）３４５まで引き出され、基板上面３００Ａで接続するＩＣチップと接続されるようになっている。

【０００３】

【発明が解決しようとする課題】しかしながら、このようなチップコンデンサを配線基板に搭載、接続すると、そのための工数がかかる。また、基板裏面やＩＣチップの周囲にチップキャパシタを配置することになるため、ＩＣチップからチップキャパシタまでの距離が長くなり、その途中の配線にノイズが侵入する。そこで、コンデンサを配線基板と一体に、しかもＩＣチップの近傍に

形成するため、樹脂絶縁層の一部を誘電体層としたコンデンサを配線基板中に形成することが考えられる。

【０００４】しかし、薄い誘電体層を広い面積の電極層で挟んだコンデンサの構造を、例えば、図２２における樹脂絶縁層３２０と配線層３１５，３２５で構成するなど、樹脂絶縁層と配線層で実現しようとすると、ショートなどの不具合が生じやすく、配線基板の歩留まりが大きく低下する。また、コア基板に樹脂絶縁層や配線層等を形成して付加価値が付いた状態で、形成したコンデンサの不具合が発見されることとなるため、不具合品の廃棄に伴う損失金額も大きくなる。

【０００５】本発明は、かかる問題点に鑑みてなされたものであって、搭載するＩＣチップの近くにコンデンサを内蔵し、しかも製造容易で、歩留まりが高く、製造工程中にコンデンサの不具合が発見されても損失金額が少ない構造とした配線基板、およびそのような配線基板に用いるコア基板、さらには、このコア基板の容易かつ安価な製造方法を提供することを目的とする。

【０００６】

【課題を解決するための手段、作用及び効果】そしてその解決手段は、コア基板と、上記コア基板の表面及び裏面に積層された１または複数の樹脂絶縁層と、上記コア基板と上記樹脂絶縁層の間及び上記樹脂絶縁層同士の間の少なくともいずれかに形成された配線層とを有する配線基板であって、上記コア基板は、樹脂および高誘電体粉末を含む複数の複合誘電体層と、上記複数の複合誘電体層と交互に積層され、これらの層間及び最下層の上記複合誘電体層の下面及び最上層の上記複合誘電体層の上面に形成され、上記複合誘電体層を挟んで対向する複数の金属層と、上記複数の複合誘電体層及び複数の金属層を貫通する貫通孔内に形成され、上記コア基板表面及びコア基板裏面まで延びる複数のスルーホール導体と、を備え、上記複数の複合誘電体層と上記複数の金属層とは、層状コンデンサを構成し、上記複数のスルーホール導体は、上記複数の金属層のうち上記層間に形成された内側金属層から１層おきに選択した第１内側金属層に直接接続する複数の第１スルーホール導体と、上記内側金属層のうち上記第１スルーホール導体とは非接続の第２内側金属層と直接接続する複数の第２スルーホール導体と、上記内側金属層のいずれとも非導通の複数の第３スルーホール導体と、を含む、配線基板である。

【０００７】本発明の配線基板では、このうちのコア基板に複合誘電体層と金属層とで構成される層状コンデンサを備えているので、ＩＣチップなどの電子部品に近い位置に静電容量の大きなコンデンサを配置できるため、ノイズ除去などの効果が良好に得られる。また、コア基板に層状コンデンサを内蔵させたので、層状コンデンサの特性やショートの有無等を検査し、合格したコア基板のみを用いて配線基板を形成、即ち樹脂絶縁層や配線層等を形成できるから、配線基板の製造において、歩留ま

りも高くできる。また、内蔵のコンデンサがショート等の不具合を生じていたとしても、樹脂絶縁層や配線層が形成されていないコア基板の状態で廃棄すればよいので、付加価値が低く不具合発生に伴う損失を低く抑えることができる。従って、安価な配線基板とすることができる。

【０００８】しかも、層状コンデンサの電極をなす金属層の電位をコア基板の表面、さらには裏面で取り出せるようにするために、所望の金属層と導通するスルーホール導体をコア基板に形成してある。具体的には、上記複数の金属層のうち、コア基板表面および裏面に位置する金属層を除いた内層に位置する金属層、つまり層間に形成された内層金属層の電位を、コア基板の表面および裏面まで導く第１スルーホール導体及び第２スルーホール導体を備える。また、内層金属層に接続しない第３スルーホール導体も含まれている。このようにこの配線基板では、３種のスルーホール導体がコア基板の表面および裏面にまで延びているので、このコア基板の裏面側に形成した配線層と表面側に形成した配線層とを、このスルーホール導体で容易に接続できる。従って、例えば、裏面側で裏面側の配線層とマザーボードなどの他の配線基板とを接続し、表面側で表面側の配線層とＩＣチップなどの電子部品とを接続すると、このスルーホール導体を通じて、他の配線基板と電子部品とを接続することができる。

【０００９】しかも、第１スルーホール導体と第２スルーホール導体の間には層状コンデンサが並列に形成されるので、この第１，第２スルーホール導体にそれぞれ電源配線と接地配線とを接続することで、この電源配線と接地配線との間のノイズを容易かつ確実に除去しつつ、マザーボードなどの他の配線基板から電子部品に電力を供給することができる。また、前記層状コンデンサの金属層から前記配線基板の電子部品搭載面（表面）まで延びる配線は、スタックドビアを含むことを特徴とすると良い。ＩＣチップ等とコンデンサの電極（金属層）とを結ぶ配線は、できるだけ短く、太い配線とすることで配線の持つインダクタンスが低減でき、ノイズの侵入を抑制できるからである。

【００１０】ここで、複合誘電体層に含まれる樹脂としては、誘電率や耐熱性等を考慮して選択すればよく、例えば、エポキシ樹脂、ポリイミド樹脂、ＢＴ樹脂等の樹脂が挙げられる。また、高誘電体粉末としては、高い誘電率を有する物質の粉末であればよいが、例えば、$BaTiO_3$、$PbTiO_3$、$PbZrO_3$、$Pb(Ti,Zr)O_3$（いわゆるＰＺＴ）、$Pb(Mn,Nb)O_3$、$SrTiO_3$、$CaTiO_3$、$MgTiO_3$等の高誘電率セラミックの粉末等が挙げられる。さらに、複合誘電体層の誘電率を上げるため、例えば、Ａｇ，Ａｕ，Ｃｕ，Ａｇ－Ｐｄ，Ｎｉ，Ｗ，Ｍｏ等の金属粉末を含めることもできる。

【００１１】他の解決手段は、コア基板と、上記コア基板の表面および裏面に積層された１または複数の樹脂絶縁層と、上記コア基板と上記樹脂絶縁層の間及び上記樹脂絶縁層同士の間の少なくともいずれかに形成された配線層とを有する配線基板であって、上記コア基板は、中心基板と、この中心基板の表面および裏面にそれぞれ形成され、樹脂および高誘電体粉末を含む１または複数の複合誘電体層とこれを挟んで対向する複数の金属層とを交互に積層してなる層状コンデンサと、上記表面側の層状コンデンサ、上記中心基板、上記裏面側の層状コンデンサを貫通する貫通孔内に形成され、上記コア基板表面及びコア基板裏面まで延びる複数のスルーホール導体と、を備え、上記複数のスルーホール導体は、上記表面側の層状コンデンサに含まれる上記複数の金属層のうち、表面側層状コンデンサの一方の電極をなす１または複数の金属層に直接接続し、上記裏面側の層状コンデンサに含まれる上記複数の金属層のうち、裏面側層状コンデンサの一方の電極をなす１または複数の金属層に直接接続する第１スルーホール導体と、上記表面側の層状コンデンサに含まれる上記複数の金属層のうち、表面側層状コンデンサの他方の電極をなす１または複数の金属層に直接接続し、上記裏面側の層状コンデンサに含まれる上記複数の金属層のうち、裏面側層状コンデンサの他方の電極をなす１または複数の金属層に直接接続する第２スルーホール導体と、上記表面側層状コンデンサ及び裏面側層状コンデンサの電極のいずれとも非導通の第３スルーホール導体と、を含む配線基板である。

【００１２】本発明の配線基板によれば、中心基板の表面及び裏面に層状コンデンサを有する。このため、ＩＣチップなどの電子部品に近い位置にコンデンサを配置できるので、ノイズ除去などの効果が良好に得られる。また、コア基板に層状コンデンサを形成しているので、層状コンデンサの特性やショートの有無等を検査し合格したコア基板のみを用いて配線基板を形成できるから、配線基板の製造において、歩留まりも高くできる。また、樹脂絶縁層や配線層が形成されていないコア基板の状態で廃棄すればよいので、付加価値が低く不具合発生に伴う損失を低く抑えることができる。従って、安価な配線基板とすることができる。

【００１３】しかも、層状コンデンサの電極をなす金属層の電位は、第１スルーホール導体及び第２スルーホール導体によってコア基板の表面および裏面で取り出せる。また、層状コンデンサの電極のいずれとも非導通の第３スルーホール導体も含まれている。このようにして、この配線基板では、スルーホール導体がコア基板の表面および裏面に延びているので、このコア基板の裏面側に形成した配線層と表面側に形成した配線層とを、このスルーホール導体で容易に接続できる。従って、例えば、裏面側で裏面側の配線層とマザーボードなどの他の配線基板とを接続し、表面側で表面側の配線層とＩＣチ

ップなどの電子部品とを接続すると、このスルーホール導体を通じて、他の配線基板と電子部品とを接続することができる。

【００１４】しかも、第１スルーホール導体と第２スルーホール導体の間には層状コンデンサが並列に形成されるので、この第１，第２スルーホール導体にそれぞれ電源配線と接地配線とを接続することで、この電源配線と接地配線との間のノイズを容易かつ確実に除去しつつ、マザーボードなどの他の配線基板から電子部品に電力を供給することができる。さらに、この配線基板では、中心基板の表面および裏面に層状コンデンサを形成しているので、中心基板の材質や厚さを適宜選定することで、コア基板、さらには配線基板の剛性を中心基板に坦持させることができるので、配線基板の剛性を容易に確保することができる。

【００１５】ここで、中心基板としては、耐熱性、機械的強度、可撓性、加工の容易さ等を考慮して選択すればよいが、例えば、ガラス織布、ガラス不織布などのガラス繊維とエポキシ樹脂、ポリイミド樹脂、ＢＴ樹脂等の樹脂とのガラス繊維－樹脂複合材料や、ポリアミド繊維などの有機繊維と樹脂との複合材料、連続気孔を有するＰＴＦＥなど３次元網目構造のフッ素系樹脂にエポキシ樹脂等の樹脂を含浸させた樹脂－樹脂複合材料などを用いることができる。これらの樹脂含む材料を中心基板に用いた場合には、レーザ加工やドリル加工で、層状コンデンサと共に中心基板に容易に穿孔できる点で好ましい。また、銅、黄銅、ニッケル、アルミニウム、銅－インバー－銅クラッド、銅－モリブデン－銅クラッドなどからなる金属板を用いても良い。これらの金属板を中心基板として用いる場合には、中心基板をコンデンサの電極の１つとして用いる構造を採用することもできる。また、前記層状コンデンサの金属層から前記配線基板の電子部品搭載面（表面）まで延びる配線は、スタックドビアを含むことを特徴とすると良い。ＩＣチップ等とコンデンサの電極（金属層）とを結ぶ配線は、できるだけ短く、太い配線とすることで配線の持つインダクタンスが低減でき、ノイズの侵入を抑制できるからである。

【００１６】さらに、上記いずれかに記載の配線基板であって、前記複数のスルーホール導体は、内部にプラグ材が充填され、前記コア基板表面及びコア基板裏面にそれぞれ閉塞部を備え、上記閉塞部のうち、上記コア基板表面側の表面側閉塞部上には、上記コア基板の表面に積層された前記樹脂絶縁層を貫通する閉塞部上ビア導体を備える配線基板とするのが好ましい。

【００１７】このようにスルーホール導体内にプラグ材を充填し閉塞部を形成し、閉塞部上ビア導体を形成することで、スルーホール導体を通じて層状コンデンサの電極をより短い距離で、従って、低抵抗かつ低インダクタンスで配線基板表面まで導くことができ、ノイズの侵入をさらに防止することができる。

【００１８】さらに、上記の配線基板であって、前記閉塞部上ビア導体にさらにビア導体を積み重ねてなる配線基板とするのが好ましい。このように、閉塞部上ビア導体にさらにビア導体を積み重ねるスタックドビアの構造とすると、閉塞部上ビア導体とその上のビア導体とを直接接続できる。故に、スルーホール導体を通じて層状コンデンサの電極をさらに短い距離で、従って、さらに低抵抗かつ低インダクタンスで配線基板表面まで導くことができ、ノイズの侵入を防止することができる。

【００１９】さらに、上記配線基板であって、前記コア基板のうち、上記配線基板の表面に搭載されるＩＣチップの搭載位置を厚さ方向に投影してなるＩＣ対応部には、前記３種のスルーホール導体のうち、前記第１スルーホール導体及び第２スルーホール導体が形成され、前記第３スルーホール導体は形成されないか、またはこのＩＣ対応部に形成された前記第１スルーホール導体と第２スルーホール導体の和よりも少数形成され、上記ＩＣ対応部の周縁部には、上記第３スルーホール導体が上記ＩＣ対応部よりも多く形成されている配線基板とすると良い。

【００２０】前述したように、ＩＣチップの電源端子や接地端子と配線基板に形成するコンデンサの電極、あるいは電源配線や接地配線とは、できるだけ短い距離で接続することが望ましい。配線を低抵抗、低インダクタンスとして、ノイズの侵入を防止するためである。一方、信号端子に接続する信号配線は、コンデンサとの接続や電源配線、接地配線ほど低抵抗、低インダクタンスであることは求められていない。

【００２１】これに対し、本発明の配線基板では、信号配線等に用いる第３スルーホール導体は、ＩＣ対応部よりもその周縁部に多く形成されている。つまり、多くの第３スルーホール導体は、ＩＣ対応部の周縁部に形成されている。このため、ＩＣチップの直下に位置するＩＣ対応部において、第１スルーホール導体や第２スルーホール導体を形成するにあたって、第３スルーホール導体を配置を考慮する必要が無い、あるいは必要が少なくなる。従って、第１スルーホール導体や第２スルーホール導体を適切な位置に配置して、これらとＩＣチップの電源端子や接地端子との間を、ごく短い距離で結ぶことができる。これにより、第１，第２スルーホール導体とＩＣチップの電源端子や接地端子との間の抵抗やインダクタンスをできるだけ低くして、この部分で侵入するノイズを低減することができる。さらに、この配線基板では、第１，第２スルーホール導体の間に層状コンデンサが形成されているので、この点でもノイズを低減させることができる。なお、上記から容易に理解できるように、ＩＣ対応部の周縁部に、すべての第３スルーホール導体を形成し、ＩＣ対応部内に、第３スルーホール導体を形成しないようにしても良く、このようにするのがさらに好ましい。

【００２２】さらに、他の解決手段は、その表面及び裏面に１または複数の樹脂絶縁層及び配線層を形成して配線基板とするためのコア基板であって、樹脂および高誘電体粉末を含む複数の複合誘電体層と、上記複数の複合誘電体層と交互に積層され、これらの層間及び最下層の上記複合誘電体層の下面及び最上層の上記複合誘電体層の上面に形成され、上記複合誘電体層をそれぞれ挟んで対向する複数の金属層と、上記複数の複合誘電体層及び複数の金属層を貫通する貫通孔内に形成され、上記コア基板表面及びコア基板裏面（最下層の複合誘電体層の下面及び上記最上層の複合誘電体層の上面）まで延びる複数のスルーホール導体と、を備え、上記複数の複合誘電体層と上記複数の金属層は、層状コンデンサを構成し、上記複数のスルーホール導体は、上記複数の金属層のうち上記層間に形成された内側金属層から１層おきに選択した第１内側金属層に直接接続する第１スルーホール導体と、上記内側金属層のうち上記第１スルーホール導体とは非接続の第２内側金属層と直接接続する第２スルーホール導体と、上記内側金属層のいずれとも非導通の第３スルーホール導体と、を含む、コア基板である。

【００２３】本発明によれば、ショート等の不具合を生じやすいコンデンサをコア基板に内蔵させたことにより、コア基板が完成した時点で層状コンデンサの静電容量やショートの有無等を判定することができる。従って、配線基板を形成するにあたり、所定規格に合格したコア基板のみを使用することができるので、配線基板全体の歩留まりを高くすることができる。また、樹脂絶縁層や配線層を形成して付加価値が付いた状態で、層状コンデンサのショートや容量不良などの不具合が発見されて廃棄される場合を少なくできるので、損失金額も抑制できる。

【００２４】しかも、層状コンデンサの電極をなす金属層の電位をコア基板の表面、さらには裏面で取り出して、コア基板の表面側及び裏面側に形成する配線層と容易に接続できるようにするために、所定の内側金属層と導通するスルーホール導体をコア基板に形成してある。具体的には、上記複数の金属層のうちコア基板表面および裏面に位置する金属層を除いた内層に位置する金属層、つまり層間に形成された内層金属層の電位を、コア基板の表面および裏面まで導く第１スルーホール導体及び第２スルーホール導体を備える。また、内層金属層に接続しない第３スルーホール導体も含まれている。このようにこのコア基板では、３種のスルーホール導体がそれぞれコア基板の表面および裏面にまで延びているので、このコア基板の裏面側に形成した配線層と表面側に形成した配線層とを、このスルーホール導体で容易に接続できる。しかも、第１スルーホール導体と第２スルーホール導体の間には層状コンデンサが並列に形成されるので、この第１，第２スルーホール導体にそれぞれ電源配線と接地配線とを接続することで、この電源配線と接地配線との間のノイズを容易かつ確実に除去することができる。

【００２５】さらに他の解決手段は、その表面及び裏面に１または複数の樹脂絶縁層及び配線層を形成して配線基板とするためのコア基板であって、中心基板と、この中心基板の表面および裏面にそれぞれ形成され、樹脂および高誘電体粉末を含む１または複数の複合誘電体層とこれを挟んで対向する複数の金属層とを交互に積層してなる層状コンデンサと、上記表面側の層状コンデンサ、上記中心基板、上記裏面側の層状コンデンサを貫通する貫通孔内に形成され、上記コア基板表面及びコア基板裏面まで延びる複数のスルーホール導体と、を備え、上記複数のスルーホール導体は、上記表面側の層状コンデンサに含まれる上記複数の金属層のうち、表面側層状コンデンサの一方の電極をなす１または複数の金属層に直接接続し、上記裏面側の層状コンデンサに含まれる上記複数の金属層のうち、裏面側層状コンデンサの一方の電極をなす１または複数の金属層に直接接続する第１スルーホール導体と、上記表面側の層状コンデンサに含まれる上記複数の金属層のうち、表面側層状コンデンサの他方の電極をなす１または複数の金属層に直接接続し、上記裏面側の層状コンデンサに含まれる上記複数の金属層のうち、裏面側層状コンデンサの他方の電極をなす１または複数の金属層に直接接続する第２スルーホール導体と、上記表面側層状コンデンサ及び裏面側層状コンデンサの電極のいずれとも非導通の第３スルーホール導体と、を含むコア基板である。

【００２６】本発明のコア基板によれば、中心基板の表面及び裏面に層状コンデンサを有する。このため、ＩＣチップなどの電子部品に近い位置にコンデンサを配置できるのでノイズ除去などの効果が良好に得られる。また、コア基板に層状コンデンサを形成しているので、層状コンデンサの特性やショートの有無等を検査し合格したコア基板のみを用いて配線基板を形成できるから、配線基板の製造において、歩留まりも高くできる。また、層状コンデンサがショート等の不具合を生じていたとしても、樹脂絶縁層や配線層が形成されていないコア基板の状態で廃棄すればよいので、付加価値が低く不具合発生に伴う損失を低く抑えることができる。しかも、このコア基板では、３種のスルーホール導体がそれぞれコア基板の表面および裏面にまで延びているので、このコア基板の裏面側に形成した配線層と表面側に形成した配線層とを、このスルーホール導体で容易に接続できる。

【００２７】さらに、上記のコア基板であって、前記中心基板は、前記複合誘電体層よりも厚いコア基板とするのが好ましい。このように中心基板を複合誘電体層よりも厚くすると、中心基板の剛性が高くなり、コア基板ひいてはこれを用いた配線基板の剛性を、中心基板に担持させることができ、取り扱いの容易なコア基板や配線基板とすることができる。

【００２８】さらに、上記のコア基板であって、前記中心基板の表面側に形成された前記複合誘電体層及び金属層と、前記中心基板の裏面側に形成された前記複合誘電体層及び金属層とは、層数、材質、及び対応する各層の厚さが等しくされているコア基板とするのが好ましい。中心基板の表面側と裏面側で、複合誘電体層や金属層の層数、材質、対応する各層の厚さが異なると、中心基板の両面で熱膨張率やコア基板形成の際の収縮などがアンバランスになり、コア基板に反りが生じることがある。本発明では、層数、材質、対応する各層の厚さが等しくされているので、コア基板の反りを生じさせることが無く、安定した形状のコア基板とすることができる。

【００２９】さらに、上記のコア基板であって、前記複数のスルーホール導体は、内部にプラグ材が充填され、前記コア基板表面及びコア基板裏面にそれぞれ閉塞部を備えるコア基板とするのが好ましい。スルーホール導体に閉塞部を形成しておくと、この閉塞部上にさらにビア導体（閉塞部上ビア導体）を形成することができるようになる。この閉塞部上ビア導体を形成すると、スルーホール導体とビア導体との間に配線層が介在せず、両者が直接接続するため、低抵抗、低インダクタンスの配線と実現することができる。

【００３０】さらに、上記いずれかに記載のコア基板であって、コア基板の平面方向中央部には、前記３種のスルーホール導体のうち、前記第１スルーホール導体及び第２スルーホール導体が形成され、前記第３スルーホール導体は形成されないか、この中央部に形成された前記第１スルーホール導体と第２スルーホール導体の和よりも少数形成されており、コア基板の平面方向周縁部には、上記第３スルーホール導体が上記中央部よりも多数形成されているコア基板とすると良い。

【００３１】配線基板にＩＣチップを搭載する場合、一般に配線基板の中央部にＩＣチップを搭載する。ところで前述したように、ＩＣチップの電源端子や接地端子と配線基板に形成するコンデンサ、あるいは電源配線や接地配線とは、できるだけ短い距離で接続することが望ましい。配線を低抵抗、低インダクタンスとして、ノイズの侵入を防止するためである。一方、信号端子に接続する信号配線は、コンデンサや電源配線、接地配線ほど低抵抗、低インダクタンスであることは求められていない。

【００３２】これに対し、本発明のコア基板では、信号配線等に用いる第３スルーホール導体は、中央部よりもその周縁部に多く形成されている。つまり、多くの第３スルーホール導体は、周縁部に形成されている。このため、ＩＣチップの直下に位置する中央部において、第１スルーホール導体や第２スルーホール導体を形成するにあたって、第３スルーホール導体を配置を考慮する必要が無い、あるいは必要が少なくなる。従って、第１スルーホール導体や第２スルーホール導体を適切な位置に配置して、これらとＩＣチップの電源端子や接地端子との間を、ごく短い距離で結ぶことができる。これにより、層状コンデンサの各電極に接続する第１，第２スルーホール導体とＩＣチップの電源端子や接地端子との間の抵抗やインダクタンスをできるだけ低くして、この部分で侵入するノイズを低減させることができる。

【００３３】さらに他の解決手段は、層状コンデンサを構成する、樹脂および高誘電体粉末を含む１または複数の複合誘電体層と、上記複合誘電体層をそれぞれ挟んで対向する複数の金属層と、を備えるコア基板の製造方法であって、金属箔と、半硬化の樹脂と高誘電体粉末とを含む半硬化複合誘電体層と、補強フィルムとをこの順に有する三層フィルムを形成する三層フィルム形成工程と、上記三層フィルムの金属箔を所定パターンに成形し、パターン化金属箔と半硬化複合誘電体層と補強フィルムとからなるパターン化三層フィルムを形成するパターン化三層フィルム形成工程と、上記補強フィルムが剥がされた１の上記三層フィルムと１または複数の上記パターン化三層フィルムとを、上記１の三層フィルムの金属箔を最下層として半硬化複合誘電体層とパターン化金属箔とが交互に重なるように積層し、最上面の上記半硬化複合誘電体層に金属箔を重ね、熱プレスして、積層板を形成する積層板形成工程と、上記積層板の表裏面を貫通する複数の貫通孔を形成する貫通孔形成工程と、上記貫通孔内にスルーホール導体を形成すると共に、上記積層体の表裏面に表面側金属層及び裏面側金属層を形成する表裏面金属層形成工程と、を備えることを特徴とするコア基板の製造方法である。

【００３４】本発明のコア基板の製造方法では、三層フィルムおよびパターン化三層フィルムを予め形成しておき、積層板形成工程で補強フィルムを剥がした三層フィルム、パターン化三層フィルムおよび金属箔を順に積層して熱プレスして、一挙に積層板を形成する。従って、ビルドアップ多層配線基板を形成する場合のように、１層ずつ順に複合誘電体層や金属層を形成する必要はなく、三層フィルムやパターン化三層フィルムを予め別々に形成しておき、積層して一挙に積層板を形成できるので、コア基板製造の工程が単純で短くなり、コア基板を安価に製造できる。また、補強フィルムを有する三層フィルム及びパターン化三層フィルムを用いたので、複合誘電体層や金属箔あるいはパターン化金属箔のハンドリング容易であり、たとえ金属箔や半硬化複合誘電体層の厚さを薄くした場合でも作業性が良いため、容易にコア基板を製造することができる。また、半硬化複合誘電体層が補強フィルムで覆われているため、半硬化のために粘着性がある状態の半硬化複合誘電体層にゴミなどが付着することをも防止し、ゴミによる不具合発生も防止することができる。

【００３５】ここで、前記コア基板の製造方法において、前記三層フィルム形成工程は、前記樹脂と高誘電体

粉末とを含む複合誘電体ペーストを前記金属箔に塗布し、未硬化複合誘電体層に補強フィルムを貼り付け、加熱して上記樹脂を半硬化させて前記三層フィルムを形成することを特徴とするコア基板の製造方法とすると良い。金属箔に複合誘電体ペーストを塗布するため、三層フィルムの段階で、あるいは積層板とした後でも、金属箔やパターン化金属箔と複合誘電体層との密着性が良好となるからである。また、両者間に空気やゴミ等が入り難いため不具合の発生を防止することもできる。

【００３６】さらに、積層する際に接着剤を用いても良い。即ち、前記コア基板の製造方法において、前記積層板形成工程は、前記１の三層フィルムの金属箔を最下層として半硬化複合誘電体層とパターン化金属箔とを接着剤層を介して交互に重なるように積層し、最上面の前記半硬化複合誘電体層に金属箔を接着剤層を介して重ね、熱プレスすることを特徴とするコア基板の製造方法としても良い。このようにすると、複合誘電体層と金属箔を確実に接着させた積層体とすることができるからである。一方、接着剤層を介さずに積層した場合には、接着剤を用いた場合に比して層状コンデンサの静電容量を大きくすることができる。

【００３７】さらに、上記のコア基板の製造方法であって、前記貫通孔形成工程は、前記パターン化金属箔から１層おきに選択した第１パターン化金属箔が内周に露出する第１貫通孔と、上記パターン化金属箔のうち上記第１パターン化金属箔に選択されなかった残余の第２パターン化金属箔が内周に露出する第２貫通孔と、上記パターン化金属箔のいずれも内周に露出しない第３貫通孔と、を形成するコア基板の製造方法とすると良い。

【００３８】このように３種のスルーホール導体を形成すると、１層おきに第１パターン化金属箔と第２パターン化金属箔とは複合誘電体層を挟んで対向した状態となり、積層された層状コンデンサを容易に形成できるからである。

【００３９】さらに他の解決手段は、中心基板と、この中心基板の表面及び裏面のうち少なくともいずれかに、層状コンデンサを構成する、樹脂および高誘電体粉末を含む１または複数の複合誘電体層と、これを挟んで対向する複数の金属層と、を備えるコア基板の製造方法であって、金属箔と、半硬化の樹脂と高誘電体粉末とを含む半硬化複合誘電体層と、補強フィルムとをこの順に有する三層フィルムを形成する三層フィルム形成工程と、表面及び裏面のうち少なくともいずれかに所定パターンの金属層を備える中心基板の上記金属層に、上記補強フィルムが剥がされた上記三層フィルムの半硬化複合誘電体層を重ね、熱プレスして、積層板を形成する積層板形成工程と、上記積層板の表裏面を貫通する複数の貫通孔を形成する貫通孔形成工程と、上記貫通孔内にスルーホール導体を形成すると共に、上記積層板の表裏面に表面側金属層及び裏面側金属層を形成する表裏面金属層形成工程と、を備えることを特徴とするコア基板の製造方法である。

【００４０】本発明のコア基板の製造方法では、三層フィルムを予め形成しておき、積層板形成工程で補強フィルムが剥がされた三層フィルムを中心基板の表裏面のうち少なくともいずれかに積層し熱プレスして、一挙に積層板を形成する。従って、ビルドアップ多層配線基板を形成する場合のように、中心基板の表面や裏面に１層ずつ順に複合誘電体層や金属層を形成する必要はなく、三層フィルムを予め別に形成しておき、積層して一挙に積層板を形成できるので、コア基板製造の工程が単純で短くなり、コア基板を安価に製造できる。また、補強フィルムを有する三層フィルムを用いたので、複合誘電体層や金属層のハンドリング容易であり、たとえ金属箔や（半硬化）複合誘電体層の厚さを薄くした場合でも、作業性が良いため、容易にコア基板を製造することができる。また、半硬化複合誘電体層が補強フィルムで覆われているため、半硬化のために粘着性がある状態の半硬化複合誘電体層にゴミなどが付着することをも防止し、ゴミによる不具合発生も防止することができる。

【００４１】ここで、前記コア基板の製造方法において、前記三層フィルム形成工程は、前記樹脂と高誘電体粉末とを含む複合誘電体ペーストを前記金属箔に塗布し、未硬化複合誘電体層に補強フィルムを貼り付け、加熱して上記樹脂を半硬化させて前記三層フィルムを形成することを特徴とするコア基板の製造方法とすると良い。金属箔に複合誘電体ペーストを塗布するため、三層フィルムの段階で、あるいは積層板とした後でも、金属箔と複合誘電体層との密着性が良好となるからである。また、両者間に空気やゴミ等が入り難いため不具合の発生を防止することもできる。

【００４２】さらに、他の解決手段は、中心基板と、この中心基板の表面及び裏面のうち少なくともいずれかに、層状コンデンサを構成する、樹脂および高誘電体粉末を含む複数の複合誘電体層と、上記複合誘電体層をそれぞれ挟んで対向する複数の金属層と、を備えるコア基板の製造方法であって、金属箔と、半硬化の樹脂と高誘電体粉末とを含む半硬化複合誘電体層と、補強フィルムとをこの順に有する三層フィルムを形成する三層フィルム形成工程と、上記三層フィルムの金属箔を所定パターンに成形し、パターン化金属箔と半硬化複合誘電体層と補強フィルムとからなるパターン化三層フィルムを形成するパターン化三層フィルム形成工程と、表面及び裏面のうち少なくともいずれかに所定パターンの金属層を備える中心基板の上記金属層上に、上記補強フィルムが剥がされた１または複数の上記パターン化三層フィルムを、上記金属層またはパターン化金属箔と半硬化複合誘電体層とが重なるように積層し、最上面の上記パターン化金属箔上に上記補強フィルムが剥がされた１の上記三層フィルムの半硬化複合誘電体層が重なるように積層

し、熱プレスして、積層板を形成する積層板形成工程と、上記積層板の表裏面を貫通する複数の貫通孔を形成する貫通孔形成工程と、上記貫通孔内にスルーホール導体を形成すると共に、上記積層板の表裏面に表面側金属層及び裏面側金属層を形成する表裏面金属層形成工程と、を備えることを特徴とするコア基板の製造方法である。

【００４３】本発明のコア基板の製造方法では、三層フィルム及びパターン化三層フィルムを予め形成しておき、積層板形成工程で補強フィルムを剥がしたパターン化三層フィルム及び三層フィルムを中心基板の表面及び裏面のうち少なくともいずれかに積層し熱プレスして、一挙に積層板を形成する。従って、ビルドアップ多層配線基板を形成する場合のように、中心基板の表面や裏面に１層ずつ順に複合誘電体層や金属層を形成する必要はなく、三層フィルムやパターン化三層フィルムを予め別に形成しておき、積層して一挙に積層板を形成できるので、コア基板製造の工程が単純で短くなり、コア基板を安価に製造できる。また、補強フィルムを剥がした三層フィルムとパターン化三層フィルムとを積層したので、形成される層状コンデンサの静電容量を大きくすることができる。

【００４４】また、補強フィルムを有する三層フィルムやパターン化三層フィルムを用いたので、複合誘電体層や金属層のハンドリング容易であり、たとえ金属箔や半硬化複合誘電体層の厚さを薄くした場合でも、作業性が良いため、容易にコア基板を製造することができる。また、半硬化複合誘電体層が補強フィルムで覆われているため、半硬化のために粘着性がある状態の半硬化複合誘電体層にゴミなどが付着することをも防止し、ゴミによる不具合発生も防止することができる。

【００４５】

【発明の実施の形態】（実施形態１）次いで、本発明に係るコア基板、配線基板及びその製造方法の実施の形態を図面と共に説明する。図１に示すコア基板１１０は、５層の複合誘電体層１１１～１１５、これらの複合誘電体層１１１等と交互に積層され、その層間及び複合誘電体層１１１の図中下面及び複合誘電体層１１５の図中上面にそれぞれ形成されたＣｕからなる金属層１０１～１０６、及び貫通孔Ｈの内周面に形成され同じくＣｕからなるスルーホール導体１０７を備える。複合誘電体層１１１等とこれらを介して対向する金属層１０１等は、５層の誘電体層を有する層状のコンデンサＣ１を構成している。内側の各金属層（内側金属層）１０２～１０５のうち、共通電位とするもの（例えば、金属層１０３と１０５、あるいは１０２と１０４）は、例えば、第１スルーホール導体１０７Ａあるいは第２スルーホール導体１０７Ｂによって、それぞれコア基板表面１１０Ａあるいはコア基板裏面１１０Ｂの金属層１０１，１０６に導通される。つまり、内側金属層のうち１層おきに選択した第１内側金属層１０２，１０４は第１スルーホール導体１０７Ａに直接接続している。一方、選択されなかった第２内側金属層１０３，１０５は第２スルーホール導体１０７Ｂに直接接続している。また、外側の金属層１０１，１０６は、層状コンデンサＣ１を構成する電極として用いられる他、配線層として用いられる。

【００４６】なお、スルーホール導体１０７には、第３スルーホール導体１０７Ｃのように、信号配線等に用いるため、内部の金属層１０２等とは導通しないものもある。このコア基板１１０では、上記したように金属層１０２と１０４及び金属層１０１と１０６の一部が互いに導通しており、一方、金属層１０３と１０５及び金属層１０１と１０６の一部が互いに導通している。従って、これらの金属層同士が、各複合誘電体層１１１等を挟んで対向することにより、層状コンデンサＣ１をなしている。

【００４７】しかも、３種のスルーホール導体１０７Ａ，１０７Ｂ，１０７Ｃは、コア基板１１０の表面１１０Ａ及び裏面１１０Ｂまで延びているので、コア基板１１０の裏面１１０Ｂ側に形成する配線層と表面１１０Ａ側に形成する配線層とをこれらのスルーホール導体１０７を介して接続することができる。ここで、例えば第１スルーホール導体１０７Ａを電源配線に、また第２スルーホール導体１０７Ｂを接地配線に接続すると、電源電位と接地電位との間に層状コンデンサＣ１を並列に挿入したことになるので、これらの電位に重畳されるノイズを吸収することができる。一方、信号配線などは、第３スルーホール導体１０７Ｃに接続すれば、層状コンデンサＣ１と絶縁した状態で、コア基板１１０内を通すことができる。

【００４８】複合誘電体層１１１等は、いずれも厚さ５０μｍとされ、$BaTiO_3$ 粉末を３０vol％及びＣｕ粉末を２０vol％、エポキシ樹脂中に分散させたセラミック－金属－樹脂複合材料からなるもので、高誘電率（比誘電率εｒ＝約１８０００）の$BaTiO_3$ 粉末及びＣｕ粉末の混入により通常の樹脂より誘電率が高くされている（εｒ＝３０）。このため、コア基板１１０が構成（内蔵）する層状コンデンサＣ１の静電容量が比較的大きな値（静電容量３．０ｎＦ）とされている。

【００４９】次いで、配線基板１００について説明する。図２に示す配線基板１００は、このコア基板１１０の表裏面１１０Ａ，１１０Ｂに、それぞれエポキシ樹脂からなる３層の樹脂絶縁層１２１，１４１，１６１，１３１，１５１，１７１およびＣｕからなる２層の配線層１２５，１４５，１３５，１５５を形成したものである。各配線層１２５等は、樹脂絶縁層１２１等の層間に形成されると共に、下層に位置する金属層や配線層と接続するためのビア導体１２５Ｖ，１４５Ｖ，１３５Ｖ，１５５Ｖを含む。また、コア基板１１０のスルーホール導体１０７の内部には、それぞれエポキシ樹脂からなる

プラグ材１１６が充填され、金属層１０１，１０６にそれぞれ形成した閉塞部１０１Ｃ，１０６Ｃによって閉じられている。

【００５０】この配線基板１００は上記説明から容易に理解できるように、コア基板１１０に形成した層状コンデンサＣ１を内蔵しており、配線基板表面（ＩＣチップ搭載面）１００Ａに搭載するＩＣチップ（図示しない）と層状コンデンサとを極めて近い距離で接続することができる。従って、ノイズ除去を確実に行うことができる。また、樹脂配線層１２１，１４１等自身を高誘電率のものとした場合と異なり、樹脂絶縁層１２１等の層間に形成する配線層１２５，１４５，１３５，１５５のうち信号配線を、従来と同様の線幅で設計し引き回すことができる。樹脂絶縁層１２１等に、従来と同様のエポキシ樹脂を使用できるので、これらの誘電率が変わらず、従って、信号配線のインピーダンスも変わらないからである。従って、信号配線層含む配線層の設計等も容易にできる。

【００５１】さらに、閉塞部１０１Ｃ，１０６Ｃを形成し、この閉塞部１０１Ｃ，１０６Ｃ上に、この閉塞部と直接接続する閉塞部上ビア導体１２５Ｖ１，１３５Ｖ１をそれぞれ形成している。このようにすると、スルーホール導体１０７と閉塞部上ビア導体１２５Ｖ１，１３５Ｖ１とをごく短い距離で接続できるので、配線層１２５等の持つ抵抗やインダクタンスを低減させることができる。従って、特に、層状コンデンサＣ１とＩＣチップとの間の配線を短くし、低抵抗、低インダクタンスとして、ノイズの侵入を防止するのに役立つ。

【００５２】次いで、上記コア基板１１０の製造方法を説明する。まず、三層フィルム形成工程について説明する。図３（ａ）に示すように、厚さ１８μｍの銅箔１１を用意し、その上面１１Ａにエポキシ樹脂ペーストに$BaTiO_3$の粉末及びＣｕ粉末を分散させた複合誘電体ペーストを厚さ１０～１００μｍの範囲（本例では、約６０μｍ）に塗布して未硬化複合誘電体層１２Ｃを形成する。その後、表面の粘着性を維持しつつ粘度を上げるため、５０℃×６０分の乾燥を行う。

【００５３】次いで、厚さ２００μｍのポリイミドやポリエステルからなる補強フィルムＲＦを未硬化複合誘電体層の表面１２Ａに貼り付け、８０℃×６０分の条件で加熱し、銅箔１１，半硬化状態の複合誘電体層１２、補強フィルムＲＦをこの順に有する三層フィルム１０を形成する。この三層フィルム１０は、補強フィルムＲＦで補強されているので、たとえ銅箔１１及び後述するパターン化銅箔２１，３１や半硬化複合誘電体層１２の厚さが薄くても、各工程におけるハンドリングに耐える剛性を持つため、取り扱いが容易で、図１に示すような薄い金属層１０１等や薄い複合誘電体層１１１等を持つコア基板を容易に形成できる。また、この三層フィルム１０では、粘着性のある半硬化複合誘電体層１２を銅箔１１および補強フィルムＲＦで挟んだ構造となっているので、半硬化複合誘電体層１２にほこりが付着することも防止される。さらに、この三層フィルム１０では、銅箔１１上に複合誘電体ペーストを塗布して未硬化複合誘電体層１２Ｃを形成したので、銅箔１１と半硬化複合誘電体層１２との間に空気やほこりが介在せず、また両者の密着性が良好である。なお、さらにこの両者の密着性を向上させるため、銅箔１１の上面１１Ａを予め、黒化処理、針状メッキ、粗化エッチング等の手法により粗化しておくと、より好ましい。

【００５４】次いで、パターン化三層フィルム形成工程について説明する。図４（ａ）に示すように、この三層フィルム１０のうち銅箔１１の露出面１１Ｂ（図中上面）にドライフィルムＤＦを貼り、露光現像して所定パターンの開口ＤＦＯを形成する。次いで、図４（ｂ）に示すように、銅箔１１をエッチングして所定パターンの第１パターン化銅箔２１とし、ドライフィルムＤＦを剥離して、第１パターン化三層フィルム２０を形成する。同様にして、図４（ｃ）に示すように、第１パターン化三層フィルム２０とは異なる第２パターン化銅箔３１を有する第２パターン化三層フィルム３０も形成する。なお、次述する積層板形成工程において、積層した際、隣り合う半硬化複合誘電体層１２との密着性を向上させるため、パターン化銅箔２１、３１の露出面を予め、黒化処理、針状メッキ、粗化エッチング等の手法により粗化しておくと、より好ましい。

【００５５】その後、積層板形成工程において、図５（ａ）に示すように、図３（ｂ）に示す三層フィルム１０のうち補強フィルムＲＦを剥がした二層フィルム１０Ｃの銅箔１１を下（最下層）にして、同じく第１，第２パターン化三層フィルム２０，３０の補強フィルムＲＦをそれぞれ剥がした第１，第２パターン化二層フィルム２０Ｃ，３０Ｃを順に積層する。具体的には、半硬化複合誘電体層１２とパターン化銅箔２１，３１とが交互に重なるように積層する。なお、本実施形態では、第１パターン化二層フィルム２０Ｃと第２パターン化二層フィルム３０Ｃとをそれぞれ２層ずつ、交互に積層した。そして、最上面の半硬化複合誘電体層１２上に厚さ１８μｍの銅箔４１を重ね、真空中で、１８０℃×２Ｈｒ、３０ｋｇ／cm^2の条件で図中上下方向に熱プレスして、複合誘電体層のエポキシ樹脂を硬化させ、図５（ｂ）に示す積層体５０を一挙に形成する。この積層体５０は、５層の複合誘電体層１１１～１１５と所定パターンの金属層１０２～１０５が交互に積層され、その表裏面５０Ａ，５０Ｂに銅箔１１，４１を有している。

【００５６】その後、貫通孔形成工程において、図６に示すように、この積層板５０の表裏面５０Ａ，５０Ｂ間を貫通する直径６０μｍの貫通孔ＨをＹＡＧレーザの第４高調波を用いて所定位置に穿孔する。穿孔した貫通孔Ｈの内周面には、金属層１０２等の端面１０２Ｈ，１０

４Ｈあるいは１０３Ｈ，１０５Ｈが露出するものも形成されている。つまり、内層金属層１０２～１０５となるパターン化金属箔２１，３１のうち、１層おきに選択した第１パターン化金属箔２１，２１が内周に露出する第１貫通孔Ｈ１、選択されなかった第２パターン化金属層３１，３１が内周に露出する第２貫通孔Ｈ２、及びいずれのパターン化金属層２１，３１も露出しない第３貫通孔Ｈ３を形成する。なお、穿孔は、孔径や積層板の材質等を考慮して、ＹＡＧレーザの第３高調波やＣＯ２レーザ、あるいはドリルによって行っても良い。

【００５７】さらに、表裏面金属層形成工程において、貫通孔Ｈ内に公知のＰＴＨ形成手法によりスルーホール導体１０７を形成すると共に、銅箔１１，４１を利用して、所定パターンの金属層１０１，１０６を形成し、コア基板１１０を完成させる（図１参照）。なお、スルーホール導体１０７のうち例えば第１、第２スルーホール導体１０７Ａ，１０７Ｂと金属層１０２等とは、端面１０２Ｈ等で導通するため、上述したように、層状コンデンサの対向電極をなす金属層１０２等は、この第１、第２スルーホール導体１０７Ａ，１０７Ｂ等を通じて、コア基板１１０の表裏面１１０Ａ，１１０Ｂまで導かれ、それぞれ金属層１０１，１０６と導通している。

【００５８】このコア基板１１０の状態で、層状コンデンサＣ１のショート不良の有無や絶縁抵抗、あるいは、静電容量をチェックする。これにより、例えば金属層１０２と１０３とが接触してショートしている場合など、層状コンデンサＣ１がショート不良である場合、あるいは、静電容量が規格範囲外である場合などでは、コア基板１１０は不良と判断され、廃棄される。コンデンサの静電容量が大きいほどノイズ除去能力が高まるので、できるだけ静電容量を高くするのが好ましいが、そのためには、複合誘電体層１１１等の厚さを薄く、あるいは、コア基板１１０の面積（具体的には各金属層の面積）を広く、さらには、複合誘電体層の誘電率を高くするために銅粉末等の金属粉末の添加量を増加させる等の手法が考えられる。

【００５９】しかし、この手法のいずれも、コンデンサのショート不良を生じさせやすくするものであるため、層状コンデンサのショート不良が増加し、歩留まりが低下しやすくなる。これに対し、本実施形態では、コア基板１１０の状態で層状コンデンサのチェックができるので、樹脂絶縁層等が形成されておらず付加価値の比較的低いコア基板１１０の段階で不具合品を除去できるから、次述する配線基板１００の製造工程中あるいは製造後において、層状コンデンサ不良による歩留まりの低下や廃棄品による損失を低く抑えることができる。

【００６０】以降は、このコア基板１１０を通常のコア基板と同様に用いて、公知の手法により配線基板１００を形成すれば良い。具体的には、まず図７に示すように、スルーホール導体１０７の内部の貫通孔１０７Ｈにエポキシ樹脂からなるプラグ材１１６を充填し、メッキによって閉塞部１０１Ｃ，１０６Ｃを形成する。

【００６１】ついで、感光性エポキシ樹脂フィルムをコア基板１１０の表裏面１１０Ａ，１１０Ｂに貼り付け、露光現像してビアホールを形成した後に硬化させて樹脂絶縁層１２１，１３１とし、さらにセミアディティブ法によって、銅からなりビア導体１２５Ｖ，１３５Ｖを含む配線層１２５，１３５を形成する（図８参照）。

【００６２】その後は、同様にして樹脂絶縁層１４１，１５１及びビア導体１４５Ｖ，１５５Ｖを含む配線層１４５，１５５を形成し、さらに、ソレダーレジストの役割を果たす樹脂絶縁層１６１，１７１を形成して配線基板１００が完成する（図２参照）。

【００６３】上記の説明から容易に理解できるように、本実施形態では、積層体５０を形成するのに、三層フィルム１０やパターン化三層フィルム２０，３０を用いたため、複合誘電体層１１１等や金属層１０１，１０２等を順に形成する必要が無く、必要な層数分の三層フィルム１０やパターン化三層フィルム２０等を用意し、積層して一挙に形成できるため、容易にコア基板１１０を形成することができる。また、このコア基板１１０は、層状コンデンサを内蔵しながらも、従来のコア基板を用いた場合と同様の設備や工程によって、その表裏面１１０Ａ，１１０Ｂに樹脂絶縁層１２１等や配線層１２５等を形成できるため、コンデンサを内蔵した配線基板１００が容易に形成できる。

【００６４】（変形例）次いで、上記実施形態１の変形例のコア基板５１０及び配線基板５００について、図面を参照して説明する。本変形例のコア基板５１０及び配線基板５００は、上記実施形態１のコア基板１１０及び配線基板１００と同様な材質からなり、ほぼ同様な構造を有している。但し、上記配線基板１００では、ビア導体１２５Ｖに対しビア導体１４５を平面方向にずらした位置に形成したいわゆるスタッガードビア形式で製造したが、本変形例では、ビア導体を厚さ方向に積み重ねて形成するスタックドビアの形式で形成している。また、本変形例のコア基板の形成する３種のスルーホール導体５０７Ａ，５０７Ｂ，５０７Ｃほ平面方向の配置に特徴がある点で異なるので、異なる部分を中心に説明し、同様な部分は省略あるいは簡略化して説明する。

【００６５】まず、本変形例にかかるコア基板５１０について説明する。図９の部分拡大断面図に示すようにコア基板５１０は、実施形態１のコア基板１１０と同様に、５層の複合誘電体層５１１～５１５、これらの複合誘電体層５１１等と交互に積層され、その層間及び複合誘電体層５１１の図９中下面及び複合誘電体層５１５の図９中上面にそれぞれ形成されたＣｕからなる金属層５０１～５０６、及び貫通孔Ｈの内周面に形成され同じくＣｕからなるスルーホール導体５０７を備える。複合誘電体層５１１等とこれらを介して対向する金属層５０１

等は、５層の誘電体層を有する層状のコンデンサＣ５１を構成している。なお、内側金属層５０２～５０５のうち、１層おきに選択した第１内側金属層５０２，５０４は第１スルーホール導体５０７Ａに直接接続し、それぞれコア基板表面１１０Ａあるいはコア基板裏面１１０Ｂの金属層５０１，５０６に導通されている。一方、選択されなかった第２内側金属層５０３，５０５は第２スルーホール導体５０７Ｂに直接接続して、同様に金属層５０１，５０６に導通されている。また、外側の金属層５０１，５０６は、層状コンデンサＣ５１を構成する電極として用いられる他、配線層として用いられる。

【００６６】スルーホール導体５０７には、第３スルーホール導体５０７Ｃのように、信号配線等に用いるため、内部の金属層５０２等とは導通しないものもある。このコア基板５１０では、上記したように金属層５０２と５０４及び金属層５０１と５０６の一部が互いに導通しており、一方、金属層５０３と５０５及び金属層５０１と５０６の一部が互いに導通している。従って、これらの金属層同士が、各複合誘電体層５１１等を挟んで対向することにより、層状コンデンサＣ５１をなしている。しかも、３種のスルーホール導体５０７Ａ，５０７Ｂ，５０７Ｃは、コア基板５１０の表面５１０Ａ及び裏面５１０Ｂまで延びているので、コア基板５１０の裏面５１０Ｂ側に形成する配線層と表面５１０Ａ側に形成する配線層とをこれらのスルーホール導体５０７を介して接続することができる。ここで、例えば第１スルーホール導体５０７Ａを電源配線に、また第２スルーホール導体５０７Ｂを接地配線に接続すると、電源電位と接地電位との間に層状コンデンサＣ５１を並列に挿入したことになるので、これらの電位に重畳されるノイズを吸収することができる。一方、信号配線などは、第３スルーホール導体５０７Ｃに接続すれば、層状コンデンサＣ５１と絶縁した状態で、コア基板５１０内を通すことができる。

【００６７】次いで、本変形例にかかる配線基板５００について説明する。図１１に配線基板５００の部分拡大断面図を、図１２にその平面図を、図１３にその底面図を示す。配線基板５００は、上記実施形態１とほぼ同様の断面構造を有しており、上記コア基板５１０の表裏面５１０Ａ，５１０Ｂに、それぞれエポキシ樹脂からなる３層の樹脂絶縁層５２１，５４１，５６１，５３１，５５１，５７１およびＣｕからなる２層の配線層５２５，５４５，５３５，５５５をそれぞれ形成したものである。各配線層５２５等には、樹脂絶縁層１２１等の層間に形成されると共に、下層に位置する金属層や配線層と接続するためのビア導体５２５Ｖ，５４５Ｖ，５３５Ｖ，５５５Ｖを含む。また、コア基板５１０のスルーホール導体５０７の内部には、それぞれエポキシ樹脂からなるプラグ材５１６が充填され、金属層５０１，５０６にそれぞれ形成した閉塞部５０１Ｃ，５０６Ｃによって閉じられている。

【００６８】また、この配線基板５００の表面５００Ａ側には、図１２の平面図に示すように、平面方向略中央部にＩＣチップＣＨを搭載するようになっており、中央部にはＩＣチップＣＨの端子ＣＨＢをフリップチップ接続で接続できるように、樹脂絶縁層５６１に形成した開口５６１Ｈが、略格子状に多数形成されている。この開口５６１Ｈ内には、図１１から容易に理解できるように、配線層５４５あるいはビア導体５４５Ｖが露出している。一方、配線基板５００の裏面５００Ｂ側は、図１３の底面図に示すように、樹脂絶縁層５７１の平面方向ほぼ全面に格子状に開口５７１Ｈが形成され、マザーボードなど他の配線基板との接続のため、開口５７１内にはビア導体５５５Ｖを含む配線層５５５が露出している。

【００６９】この配線基板５００も、実施形態１の配線基板１００と同様、コア基板５１０に形成した層状コンデンサＣ５１を内蔵しており、ＩＣチップ搭載面である配線基板表面５００Ａに搭載するＩＣチップＣＨと層状コンデンサＣ５１とを極めて近い距離で接続することができる。従って、ノイズ除去を確実に行うことができる。また、信号配線も従来と同様の線幅で設計し引き回すことができ、信号配線層含む配線層の設計等も容易にできる。また、閉塞部５０１Ｃ，５０６Ｃを形成し、ビア導体５２５Ｖ，５３５Ｖを閉塞部５０１Ｃ等を直接接続する閉塞部上ビア導体としているので、スルーホール導体５０７と閉塞部上ビア導体５２５Ｖ等とをごく短い距離で接続でき、配線層５２５等の持つ抵抗やインダクタンスを低減させることができる。

【００７０】さらに、この配線基板５００では、ビア導体５２５Ｖ，５３５Ｖの上にビア導体５４５Ｖ，５５５Ｖを積み重ねたスタックドビア形式としているものもある。特に、図１１に２点鎖線で示すように、配線基板５００にＩＣチップＣＨを搭載した際のＩＣチップに対応する部分、即ち、ＩＣチップＣＨを厚さ方向に投影してなるＩＣ対応部Ｑ内の第１，第２スルーホール導体５０７Ａ，５０７ＢとＩＣチップＣＨの端子ＣＨＢとを結ぶ配線について、上記のようなスタックドビア形式で形成している。このようにスタックドビアの形式にすると、特に、層状コンデンサＣ５１とＩＣチップとの間の配線を短くできるので、さらに低抵抗、低インダクタンスになりノイズの侵入を防止するのに役立つ。

【００７１】ここで、上述したように配線基板表面５００Ａ側にＩＣチップＣＨを搭載し、裏面５００Ｂ側で他の配線基板と接続するので、配線基板５００内では、開口５６１Ｈ内に露出する配線層５４５及びビア導体５４５Ｖと、開口５７１Ｈ内に露出する配線層５５５との間を結ぶ配線を形成する。そのため、コア基板５１０に、上述したように３種のスルーホール導体５０７を形成するのであるが、本変形例のコア基板５１０では、スルー

ホール導体５０７を図１０に示すようにして平面方向に配置する。なお、本図においては、第１，第２スルーホール導体５０７Ａ，５０７Ｂは黒丸で、第３スルーホール導体５０７は白丸で表して、スルーホール導体の種類による配置の違いを理解しやすく表現している。なお、本図でも、２点鎖線で囲まれた部分は、ＩＣ対応部Ｑを示す。このＩＣ対応部Ｑは、コア基板５１０のほぼ中央部に位置している。さらに、１点鎖線で示すＰＰ’断面が、図９に示す断面に相当する。

【００７２】図１０から容易に理解できるように、中央部であるＩＣ対応部Ｑ内では、３種類のスルーホール導体５０７Ａ，５０７Ｂ，５０７Ｃのうち、第１スルーホール導体５０７Ａと第２スルーホール導体５０７Ｂが数多く形成されている。これに対し、第３スルーホール導体５０７Ｃは、少数形成されているだけで、第１、第２スルーホール導体５０７Ａ，５０７Ｂの数よりも少なくなっている。一方、ＩＣ対応部Ｑの外側の周縁部には、第３スルーホール導体５０７Ｃが数多く形成されており、第３スルーホール導体５０７Ｃについてみると、ＩＣ対応部Ｑ内に形成された数よりも、その周縁部に形成された数の方が多くされている。つまり、信号配線等に用いる第３スルーホール導体５０７Ｃの多くは、ＩＣ対応部Ｑよりもその周縁部に形成される。

【００７３】このようにスルーホール導体５０７を配置するのは、以下の理由からである。即ち、ＩＣチップＣＨの端子ＣＨＢを、コア基板５１０の層状コンデンサＣ５１の各電極（金属層）５０１～５０６と、従って、第１スルーホール導体５０７Ａ及び第２スルーホール導体５０７Ｂとをできるだけ短い距離で接続するのが好ましい。このため、第１，第２スルーホール導体５０７Ａ，５０７ＢをＩＣチップＣＨの直下に位置させるのが好ましく、しかも、多数の第１，第２スルーホール導体５０７Ａ，５０７Ｂを形成して並列に接続すると、第１、第２スルーホール導体５０７Ａ等やこれらとＩＣチップとを結ぶ配線の抵抗をさらに低減させることができる。従って、ＩＣチップＣＨの直下、つまりＩＣ対応部Ｑに多数の第１、第２スルーホール導体５０７Ａ，５０７Ｂを形成するのが好ましい。一方、第３スルーホール導体５０７Ｃを用いる信号配線などは、それほど低抵抗や低インダクタンスであることを求められないので、抵抗やインダクタンスの面から言えば、必ずしもＩＣ対応部Ｑ内に形成する必要はない。従って、できるだけ第３スルーホール導体５０７ＣをＩＣ対応部Ｑの周縁部に配置することにより、第３スルーホール導体５０７Ｃを考慮する必要が少なくなり、多数の第１，第２スルーホール導体５０７Ａ等を、容易に配置することができるようになる。つまり、より低抵抗、低インダクタンスで層状コンデンサＣ５１とＩＣチップＣＨとを接続することができるようになる。

【００７４】本変形例の配線基板５００では、スルーホール導体５０７に設けた閉塞部５０１Ｃ，５０６Ｃにビア導体５２５Ｖ，５３５Ｖを直接重ねて形成しただけでなく、ビア導体５２５Ｖと５４５Ｖ、５３５Ｖと５５５Ｖとを積み重ねたスタックドビア形式で配線を形成している。このため、ＩＣチップＣＨとさらに低抵抗、低インダクタンスに接続することができる。さらに、この配線基板及びコア基板５１０では、３種のスルーホール導体５０７の配置を考慮し、中央部のＩＣ対応部Ｑでは、第１，第２スルーホール導体５０７Ａ，５０７Ｂが第３スルーホール導体５０７Ｃよりも多くなるように配置し、しかも、第３スルーホール導体５０７Ｃは、ＩＣ対応部Ｑの周縁部の形成された数が、ＩＣ対応部Ｑ内に形成されたものの数より多くなるようにしたので、第１，第２スルーホール導体５０７Ａ，５０７Ｂを多数容易に形成することができ、層状コンデンサ５１とＩＣチップＣＨとを、さらに低抵抗、低インダクタンスで接続することができる。なお、本変形例のコア基板５１０及び配線基板５００は、上記実施形態１と同様にして形成ればよい。

【００７５】（実施形態２）次に、第２の実施の形態について説明する。本実施形態のコア基板２１０は、その中心に中心基板２１１を有し、その表裏面に層状コンデンサを備えた点で実施形態１と異なるので、異なる部分を中心に説明し、同様な部分は省略あるいは簡略化して説明する。

【００７６】図１４に示す本実施形態のコア基板２１０は、ガラス繊維－エポキシ樹脂複合材料からなる厚さ６００μｍの中心基板２１１と、その表裏面２１１Ａ，２１１Ｂにそれぞれ形成された層状コンデンサＣ２１，Ｃ２２とを備える。具体的には、中心基板２１１と、厚さ５０μｍでＢａＴｉO３粉末を３０vol％及びＣｕ粉末を２０vol％エポキシ樹脂中に分散させたセラミック－金属－樹脂複合材料からなる複合誘電体層２１２，２１３と、それぞれこれを挟んで対向しＣｕからなる金属層２０１，２０３及び２０２，２０４とを備え、さらに貫通孔Ｈの内周面に形成され同じくＣｕからなるスルーホール導体２０７をも備える。複合誘電体層２１２，２１３とこれらを介して対向する金属層２０１と２０３、２０２と２０４とは、それぞれ層状のコンデンサＣ２１，Ｃ２２を構成している。内層の金属層２０１，２０２は第１スルーホール導体２０７Ａあるいは第２スルーホール導体２０７Ｂによって、それぞれコア基板表面２１０Ａあるいはコア基板裏面２１０Ｂの金属層２０３，２０４に導通される。

【００７７】つまり、第１スルーホール導体２０７Ａは、表面側の層状コンデンサＣ２１に含まれる金属層のうち、この層状コンデンサＣ２１の一方の電極をなす金属層２０３に直接接続し、さらに、裏面側の層状コンデンサＣ２２に含まれる金属層のうち、この層状コンデンサＣ２２の一方の電極をなす金属層２０２に直接接続し

ている。また、第２スルーホール導体２０７Ｂは、表面側の層状コンデンサＣ２１に含まれる金属層のうち、この層状コンデンサＣ２１の他方の電極をなす金属層２０１に直接接続し、さらに、裏面側の層状コンデンサＣ２２に含まれる金属層のうち、この層状コンデンサＣ２２の他方の電極をなす金属層２０４に直接接続している。

【００７８】また、外側の金属層２０３，２０４は、層状コンデンサＣ２１，Ｃ２２を構成する電極としても用いられる他、配線層として用いられる。なお、スルーホール導体２０７には、第３スルーホール導体２０７Ｃのように、信号配線等に用いるため、内部の金属層２０１，２０２とは導通しないものもある。しかも、３種のスルーホール導体２０７Ａ，２０７Ｂ，２０７Ｃは、コア基板２１０の表面２１０Ａ及び裏面２１０Ｂまで延びているので、コア基板２１０の裏面２１０Ｂ側に形成する配線層と表面２１０Ａ側に形成する配線層とをこれらのスルーホール導体２０７を介して接続することができる。

【００７９】このコア基板２１０は、中心基板２１１を中心として、その表面２１１Ａおよび裏面２１１Ｂに、それぞれ１層の複合誘電体層２１２，１２３及び２層の金属層２０１，２０３と２０２，２０４を形成している。しかも、表面が和と裏側に対応する層についてみると、これらの材質は同材質で、同じ厚さにされている。従って、このコア基板２０１は、これらのアンバランスによる反りが発生し難い。

【００８０】容易に理解できるように、このコア基板２１０においても、実施形態１のコア基板１１０と同様に、層状コンデンサＣ２１，Ｃ２２を内蔵しているので、このコア基板２１０にさらに樹脂絶縁層や配線層を形成して配線基板を製作した場合には、ＩＣチップのごく近傍にコンデンサを配置することとなるため、ノイズの侵入を有効に防止することができる。具体的に言うと、例えば第１スルーホール導体２０７Ａを電源配線に、また第２スルーホール導体２０７Ｂを接地配線に接続すると、電源電位と接地電位との間に層状コンデンサＣ２１，２２を並列に挿入したことになるので、これらの電位に重畳されるノイズを吸収することができる。なお、信号配線などは、第３スルーホール導体２０７Ｃに接続すれば、層状コンデンサＣ２１，２２と絶縁した状態で、コア基板２１０内を通すことができる。

【００８１】さらに、このコア基板２１０では、複合誘電体層２１２，２１３よりも厚く、ガラス繊維－エポキシ樹脂複合材料からなる中心基板２１１を用い、この表裏面２１１Ａ，２１１Ｂに金属層２０１等及び複合誘電体層２１２，２１３を形成しているので、コア基板２１０の機械的強度が高く、変形等に耐えることができるため、取り扱いがさらに容易となる。中心基板２１１の剛性が高いので、これにコア基板２１０全体の剛性を担持させることができるためである。なお、上記実施形態１では、層状コンデンサＣ１の誘電体層として、いずれもエポキシ樹脂にＢａＴｉＯ３粉末やＣｕ粉末を混入した複合誘電体層１１１～１１５を用いた。しかし、静電容量が低下するものの、例えば、複合誘電体層１１１，１１５に代えて、ＢａＴｉＯ３粉末さらにはＣｕ粉末を混入していない樹脂による誘電体層を用いるなど、層状コンデンサを構成する誘電体層の一部が高誘電体粉末を含まない材質であっても良い。

【００８２】次いで、配線基板２００について説明する。図１５に示す配線基板２００は、上記コア基板２１０の表裏面２１０Ａ，２１０Ｂに、実施形態１と同様に、エポキシ樹脂からなる３層の樹脂絶縁層２２１，２４１，２６１，２３１，２５１，２７１およびＣｕからなる２層の配線層２２５，２４５，２３５，２５５をそれぞれ形成したものである。各配線層２２５等は、樹脂絶縁層２２１等の層間に形成されると共に、ビア導体２２５Ｖ，２４５Ｖ，２３５Ｖ，２５５Ｖを含む。また、コア基板２１０のスルーホール導体２０７の内部には、それぞれエポキシ樹脂からなるプラグ材２１６が充填され、金属層２０３，２０４にそれぞれ形成した閉塞部２０３Ｃ，２０４Ｃによって閉じられている。

【００８３】この配線基板２００も、コア基板２１０に形成した層状コンデンサを内蔵しており、配線基板表面１００Ａに搭載するＩＣチップ（図示しない）と層状コンデンサとを極めて近い距離で接続することができ、ノイズ除去を確実に行うことができる。また、実施形態１と同様に、配線層２２５等を従来と同様の線幅で設計し引き回すことができる。従って、信号配線層含む配線層の設計等も容易にできる。

【００８４】さらに、閉塞部２０３Ｃ，２０４Ｃを形成し、この閉塞部２０３Ｃ，２０４Ｃ上に、ビア導体２２５Ｖ，２３５Ｖをそれぞれ形成している。このビア導体２２５Ｖ，２３５Ｖは、閉塞部２０３Ｃ，２０４Ｃと直接接続する閉塞部上ビア導体となっている。このようにすると、スルーホール導体１０７とビア導体２２５Ｖ，２３５Ｖとをごく短い距離で接続できるので、配線層２２５等の持つ抵抗やインダクタンスを低減させることができる。従って、特に、層状コンデンサＣ２１，Ｃ２２とＩＣチップとの間の配線を短くし、低抵抗、低インダクタンスとして、ノイズの侵入を防止するのに役立つ。なお、実施形態１においては、各ビア導体１２５等の位置をずらしながら形成するスタッガードビアの形式で製作してある（図２参照）が、この配線基板２００においては、図１５から容易に理解できるように、各ビア導体２２５Ｖと２４５Ｖ、２３５Ｖと２５５Ｖとは、積み重なった状態、即ちスタックドビアの形式で形成されている。このスタックドビアで形成すると、コンデンサの電極、即ち金属層２０１等を配線基板表面２００Ａまで引き出す配線の長さが短くでき、しかも、皿状のスタッガードビアと異なり、下に位置するビア導体２２５Ｖ，２

３５Ｖは導体が充填された形状となるため、配線も太く形成でき抵抗が低くなる。従って、配線の持つインダクタンスは小さくなるので、さらにノイズの侵入を抑制することができる。

【００８５】次いで、上記コア基板２１０の製造方法を説明する。三層フィルム形成工程は、実施形態１と同様（図３参照）である。一方、図１６に示すように、予め中心基板２１１の表裏面２１１Ａ，２１１Ｂにそれぞれ所定パターンの金属層２０１，２０２を形成しておく。

【００８６】その後、積層板形成工程において、図１７（ａ）に示すように、三層フィルム１０の補強フィルムＲＦを剥がした二重フィルム１０Ｃを、それぞれ金属層２０１，２０２と半硬化複合誘電体層１２とが重なるようにして積層する。その後、真空中で、１８０℃×２Ｈｒ、３０ｋｇ／ｃｍ^{2}の条件で図中上下方向に熱プレスして、複合誘電体層のエポキシ樹脂を硬化させ、一挙に図１７（ｂ）に示す積層体６０を形成する。この積層体６０は、中心基板２１１の表裏面２１１Ａ，２１１Ｂにそれぞれ所定パターンの金属層２０１，２０２、複合誘電体層２１２，２１３、および銅箔１１，１１が積層されたものである。

【００８７】その後、貫通孔形成工程において、図１８に示すように、この積層板６０の表裏面６０Ａ，６０Ｂ間を貫通する直径６０μｍの貫通孔ＨをＹＡＧレーザの第４高調波を用いて所定位置に穿孔する。穿孔した貫通孔Ｈの内周面には、金属層２０１，２０２の端面２０１Ｈ，２０２Ｈが露出するものも形成されている。つまり、金属層２０２が内周に露出する第１貫通孔Ｈ４、金属層２０１が内周に露出する第２貫通孔Ｈ５、及び金属層２０１，２０２のいずれも露出しない第３貫通孔Ｈ６を形成する。

【００８８】さらに、表裏面金属層形成工程において、貫通孔Ｈ内に公知のＰＴＨ形成手法によりスルーホール導体２０７を形成すると共に、積層板表裏面６０Ａ，６０Ｂの銅箔１１，１１を利用して、所定パターンの金属層２０３，２０４を形成し、コア基板２１０を完成させる（図１４参照）。なお、スルーホール導体２０７のうち例えば第１、第２スルーホール導体２０７Ａ，２０７Ｂと金属層２０１，２０２とは、その端面２０１Ｈ等でそれぞれ導通するため、上述したように、層状コンデンサの対向電極をなす金属層２０１，２０２は、この第１、第２スルーホール導体２０７Ａ，２０７Ｂ等を通じて、コア基板２１０の表裏面２１０Ａ，２１０Ｂまで導かれ、それぞれ金属層２０３，２０４と導通している。

【００８９】このようにしてコア基板２１０が完成したら、実施形態１と同様に、このコア基板２１０の状態で、層状コンデンサＣ２１，Ｃ２２のショート不良の有無や絶縁抵抗、あるいは、静電容量をチェックする。これにより、例えば金属層２０１と２０３とが接触してショートしている場合など、層状コンデンサのショート不良や静電容量規格外などが検出されると、不良のコア基板２１０は廃棄される。このコア基板２１０においても、上記コア基板１１０と同様に、静電容量を高くするのが好ましいため、複合誘電体層２１２等の厚さを薄くし、コア基板２１０の面積を広くし、あるいは複合誘電体層の金属粉添加量を増加させることが考えられる。しかし、これらにより、層状コンデンサのショート不良が増加し、歩留まりが低下しやすくなる。これに対し、コア基板２１０では、この状態で層状コンデンサの良否チェックができるので、付加価値の比較的低いコア基板２１０の段階で不具合品を除去できるから、次述する配線基板２００の製造工程中あるいは製造後の層状コンデンサ不良による歩留まりの低下や廃棄品による損失を低く抑えることができる。

【００９０】以降は、実施形態１と同様、このコア基板２１０を通常のコア基板と同様に用いて、公知の手法により配線基板２００を形成すれば良い。具体的には、図１９に示すように、スルーホール導体２０７の内部の貫通孔にエポキシ樹脂からなるプラグ材２１６を充填し、メッキによって閉塞部２０３Ｃ，２０４Ｃを形成する。ついで、図２０に示すように、感光性エポキシ樹脂フィルムをコア基板２１０の表裏面２１０Ａ，２１０Ｂに貼り付け、露光現像してビアホールを形成した後に硬化させて樹脂絶縁層２２１，２３１とし、さらにセミアディティブ法によって、銅からなるビア導体２２５Ｖ，２３５Ｖを含む配線層２２５，２３５を形成する。その後は、上記と同様にして樹脂絶縁層２４１，２５１及びビア導体２４５Ｖ，２５５Ｖを含む配線層２４５，２５５を形成し、さらに、ソレダーレジストの役割を果たす樹脂絶縁層２６１，２７１を形成して配線基板２００を完成させる（図１５参照）。

【００９１】なお、上記実施形態では、中心基板２１１の表面２１１Ａに金属層２０１，２０３及び複合誘電体層２１２からなる層状コンデンサＣ２１を、また、裏面２１１Ｂに金属層２０２，２０４及び複合誘電体層２１３からなる層状コンデンサＣ２２を形成した例を示したが、必要とする静電容量が小さいときなど場合に応じて、表面又は裏面のいずれかのみに層状コンデンサを形成しても良い。

【００９２】あるいはこれとは反対に、必要とする静電容量が大きいときなどには、実施形態２の変形例として図２１に示すコア基板４１０のように、中心基板２１１の表裏面に形成する層状コンデンサＣ４１，Ｃ４２の複合誘電体層をそれぞれ複数（図２１ではそれぞれ２層２１２，４１４と２１３，４１５）とし、これらと交互に金属層（図２１では金属層２０１，４０３，４０５，２０２，４０４，４０６）を形成して、所望金属層同士をスルーホール導体４０７で相互に接続し、コンデンサの静電容量を確保するようにしても良い。

【００９３】このコア基板４１０では、第１スルーホー

ル導体４０７Ａは、表面側の層状コンデンサＣ４１に含まれる金属層のうち、この層状コンデンサＣ４１の一方の電極をなす金属層４０３に直接接続し、さらに、裏面側の層状コンデンサＣ４２に含まれる金属層のうち、この層状コンデンサＣ４２の一方の電極をなす金属層２０２，４０６に直接接続している。また、第２スルーホール導体４０７Ｂは、表面側の層状コンデンサＣ４１に含まれる金属層のうち、この層状コンデンサＣ４１の他方の電極をなす金属層２０１，４０５に直接接続し、さらに、裏面側の層状コンデンサＣ４２に含まれる金属層のうち、この層状コンデンサＣ４２の他方の電極をなす金属層４０４に直接接続している。さらに、表面側の層状コンデンサ４１及び裏面側の層状コンデンサ４２の電極のいずれとも非導通の第３スルーホール導体４０７Ｃも含まれている。

【００９４】このコア基板４１０の製造方法としては、三層フィルム１０の他、所望パターンのパターン化銅箔２１，３１等を形成したパターン化三層フィルム２０，３０（図４参照）を予め用意しておく。そして、中心基板２１１の表裏面２１１Ａ，２１１Ｂに予め形成しておいた金属層２０１，２０２上に、それぞれ補強フィルムＲＦを剥がしたパターン化三層フィルム２０等を先に積層し、その後補強フィルムＲＦを剥がした三層フィルム１０を積層し、熱プレスして積層体を形成し、その後は上記と同様にして形成すればよい。

【００９５】上記の説明から容易に理解できるように、本実施形態やその変形例においても、積層体６０等を形成するのに、複合誘電体層２１２，２１３や金属層２０１，２０２等を順に形成する必要が無い。即ち、金属層２０１，２０２を形成した中心基板２１１と三層フィルム１０、さらにはパターン化三層フィルム２０等を用意し、これらを積層して一挙に形成できるため、容易にコア基板２１０，４１０を形成することができる。また、このようにして形成したコア基板２１０，４１０は、層状コンデンサを内蔵しながらも、従来のコア基板を用いた場合と同様の設備や工程によって、その表裏面２１０Ａ，２１０Ｂ，４１０Ａ等に樹脂絶縁層２２１等や配線層２２５等を形成できるため、コンデンサを内蔵した配線基板２００などが容易に形成できる。

【００９６】以上において、本発明を実施形態１，２及びその変形例に即して説明したが、本発明は上記実施形態等に限定されるものではなく、その要旨を逸脱しない範囲で、適宜変更して適用できることはいうまでもない。例えば、実施形態１では、５層の複合誘電体層を積層したコア基板１１０を示したが、必要な静電容量に応じて、層数を増やすあるいは減らす等、適宜変更することができる。また、複合誘電体層として、エポキシ樹脂に$BaTiO_3$粉末及びＣｕ粉末を分散させたものを使用したが、他の高誘電率粉末や金属粉末を使用することもできる。さらに、上記実施形態ではいずれも、補強フィルムＲＦを剥がした三層フィルム１０あるいはパターン化三層フィルム２０，３０、即ち二層フィルム１０Ｃあるいはパターン化二層フィルム２０Ｃ，３０Ｃを、銅箔１１，４１やパターン化銅箔２１，３１等に直接重ねて積層した。しかし、エポキシ樹脂等からなる接着剤を塗布あるいは接着材フィルムを配置して接着剤層を介在させて積層し、熱プレスして積層体を形成しても良い。この場合には、複合誘電体層１１１等と金属層１０２等とを確実に接着させた積層体とすることができる。

【００９７】さらに、上記実施形態等では、補強フィルムＲＦを貼り付けた三層フィルム１０及びパターン化三層フィルム２０，３０を用いたが、取り扱いその他を考慮した上で、補強フィルムＲＦを用いずに、二層フィルム１０Ｃやパターン化二層フィルム２０Ｃ，３０Ｃのみを用いるようにしても良い。

【図面の簡単な説明】

【図１】実施形態１にかかるコア基板の部分拡大断面図である。

【図２】実施形態１にかかる配線基板の部分拡大断面図である。

【図３】実施形態１にかかるコア基板及び配線基板の製造方法のうち、（ａ）は銅箔上に複合誘電体層を形成した状態、（ｂ）は補強フィルムを貼り付け３層フィルムを形成した状態を示す。

【図４】実施形態１にかかるコア基板及び配線基板の製造方法のうち、（ａ）は銅箔上に所定パターンのエッチングレジストを形成した状態、（ｂ）は銅箔をエッチングして所定パターンに成形した状態、（ｃ）は銅箔を（ｂ）と別のパターンに成型した状態を示す。

【図５】実施形態１にかかるコア基板及び配線基板の製造方法のうち、（ａ）は３層フィルムから補強フィルムを剥がして積層する様子を、（ｂ）は積層、プレスして成形された積層板を示す。

【図６】実施形態１にかかるコア基板及び配線基板の製造方法のうち、図５に示す積層板に貫通孔を形成した状態を示す。

【図７】実施形態１にかかる配線基板の製造方法のうち、図１に示すコア基板のスルーホール導体中央の透孔内に樹脂を充填し、透孔の上下にも導体を形成した透孔を塞いだ状態を示す部分拡大断面図である。

【図８】実施形態１にかかる配線基板の製造方法のうち、図７に示すコア基板の表裏面上に樹脂絶縁層及び配線層を形成した状態を示す部分拡大断面図である。

【図９】実施形態１の変形例にかかるコア基板の部分拡大断面図である。

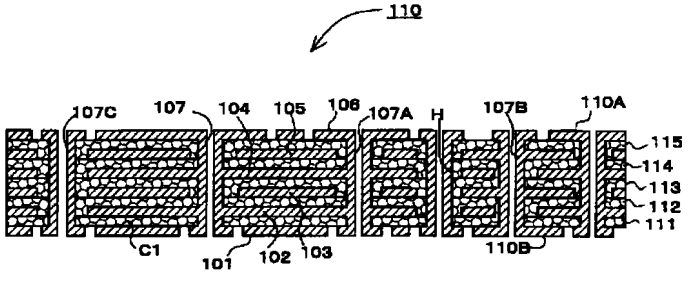
【図１０】実施形態１の変形例にかかるコア基板のスルーホール導体の配置を示す図である。

【図１１】実施形態１の変形例にかかる配線基板の部分拡大断面図である。

【図１２】実施形態１の変形例にかかる配線基板の平面

図である。
【図１３】実施形態１の変形例にかかる配線基板の底面図である。
【図１４】実施形態２にかかるコア基板の部分拡大断面図である。
【図１５】実施形態２にかかる配線基板の部分拡大断面図である。
【図１６】実施形態２にかかるコア基板及び配線基板の製造方法のうち、表裏面に所定パターンの金属層を備える中心基板の部分拡大断面図である。
【図１７】実施形態２にかかるコア基板及び配線基板の製造方法のうち、（ａ）は図１１に示す中心基板の表裏面に、それぞれ補強フィルムを剥がした３層フィルムを積層する様子を、（ｂ）は積層、プレスして成形された表裏面積層板を示す。
【図１８】実施形態２にかかるコア基板及び配線基板の製造方法のうち、図１２に示す表裏面積層板に貫通孔を形成した状態を示す。
【図１９】実施形態２にかかる配線基板の製造方法のうち、図９に示すコア基板のスルーホール導体中央の透孔内に樹脂を充填し、透孔の上下にも導体を形成した透孔を塞いだ状態を示す部分拡大断面図である。
【図２０】実施形態２にかかる配線基板の製造方法のうち、図１４に示すコア基板の表裏面上に樹脂絶縁層及び配線層を形成した状態を示す部分拡大断面図である。
【図２１】実施形態２にかかるコア基板の変形例を示す部分拡大断面図である。
【図２２】下面にチップコンデンサを搭載した従来の配線基板を示す部分拡大断面図である。
【符号の説明】
１１０，２１０，４１０，５１０　コア基板
１１０Ａ，２１０Ａ，４１０Ａ，５１０Ａ　コア基板表面
１１０Ｂ，２１０Ｂ，４１０Ｂ，５１０Ｂ　コア基板＊裏面
１００，２００，５００　配線基板
１１１，１１２，１１３，１１４，１１５，２１２，２１３，４１４，４１５，５１１，５１２，５１３，５１４，５１５　複合誘電体層
１０１，１０２，１０３，１０４，１０５，１０６，２０１，２０２，２０３，２０４，４０３，４０４，４０５，４０６，５０１，５０２，５０３，５０４，５０５，５０６　金属層
１０７，２０７，４０７，５０７　スルーホール導体
１０７Ａ，２０７Ａ，５０７Ａ　第１スルーホール導体
１０７Ｂ，２０７Ｂ，５０７Ｂ　第２スルーホール導体
１０７Ｃ，２０７Ｃ，５０７Ｃ　第３スルーホール導体
Ｃ１，Ｃ２１，Ｃ２２，Ｃ４１，Ｃ４２，Ｃ５１　層状コンデンサ
１２１，１３１，１４１，１５１，１６１，１７１，２２１，２３１，２４１，２５１，２６１，２７１，５２１，５３１，５４１，５５１，５６１　樹脂絶縁層
１２５，１３５，１４５，１５５，２２５，２３５，２４５，２５５，５２５，５３５，５４５，５５５　配線層
１２５Ｖ，１３５Ｖ，１４５Ｖ，１５５Ｖ，２２５Ｖ，２３５Ｖ，２４５Ｖ，２５５Ｖ，５２５Ｖ，５３５Ｖ，５４５Ｖ，５５５Ｖ　ビア導体
２１１　中心基板
２１１Ａ　中心基板表面
２１１Ｂ　中心基板裏面
１０　三層フィルム
１１，４１　銅箔
１２　半硬化複合誘電体層
２１，３１　パターン化銅箔
ＲＦ　補強フィルム
５０，６０　積層体

【図１】



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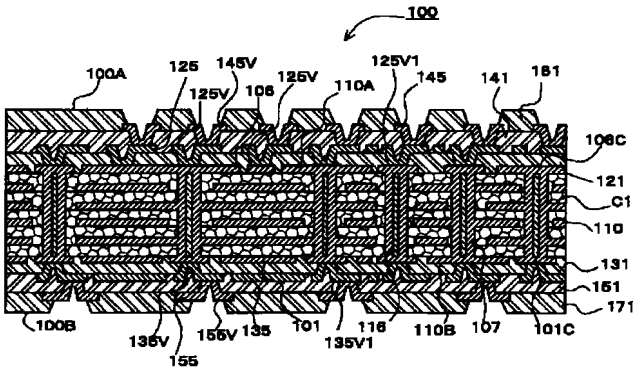

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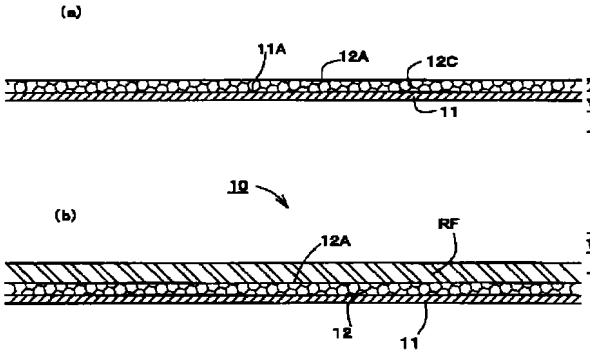

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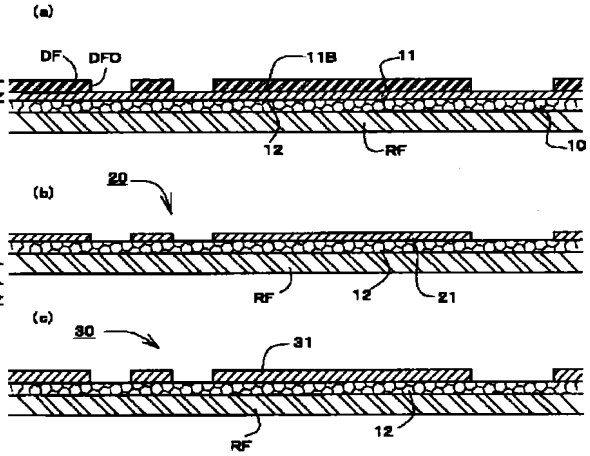

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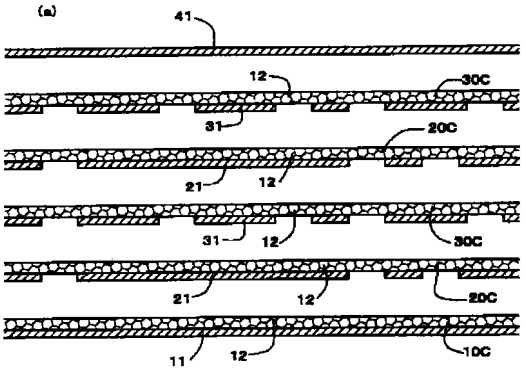

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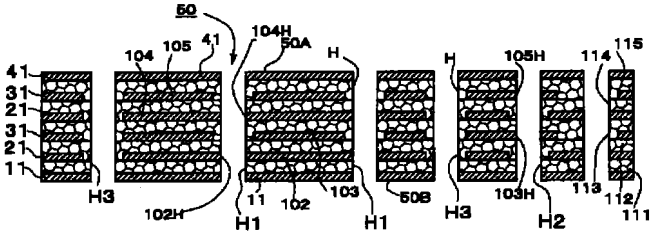

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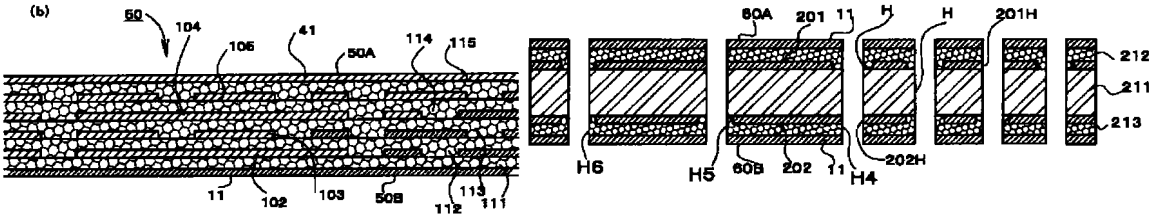

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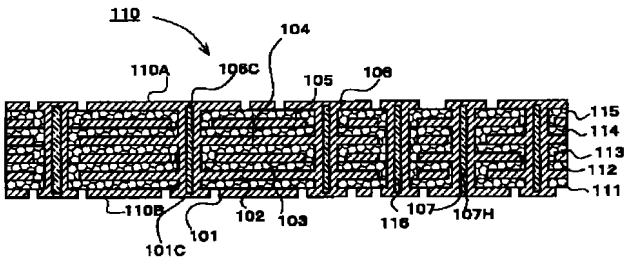

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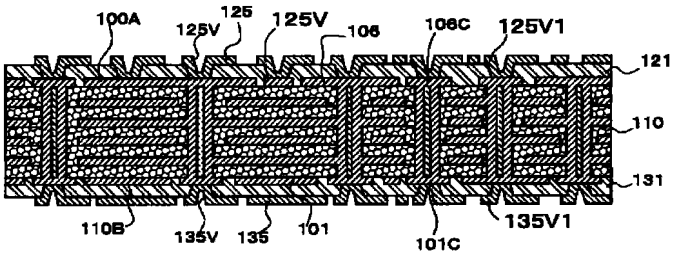

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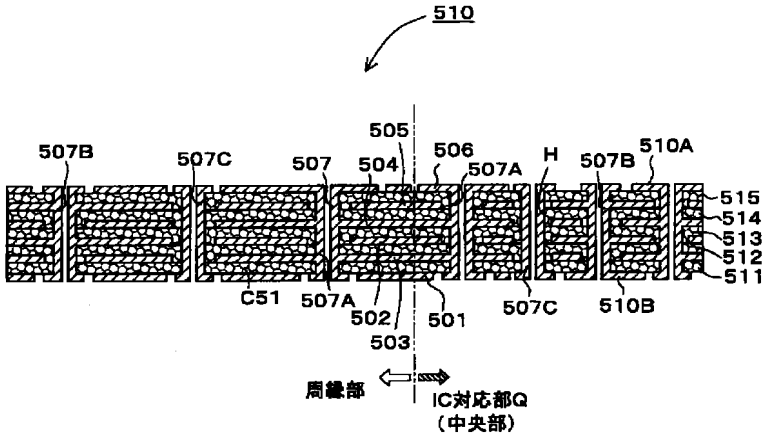

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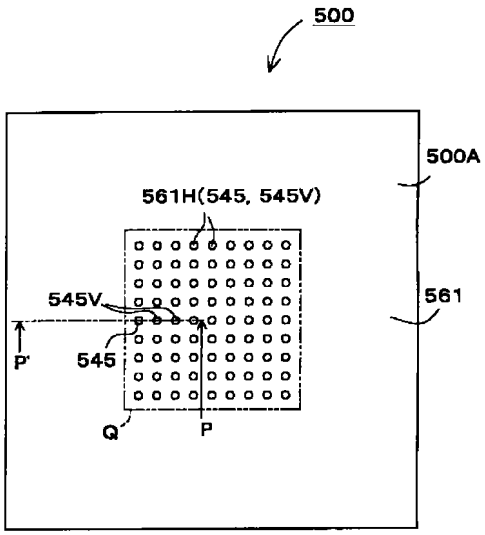

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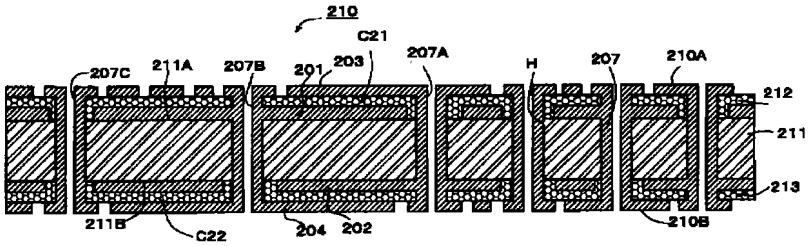

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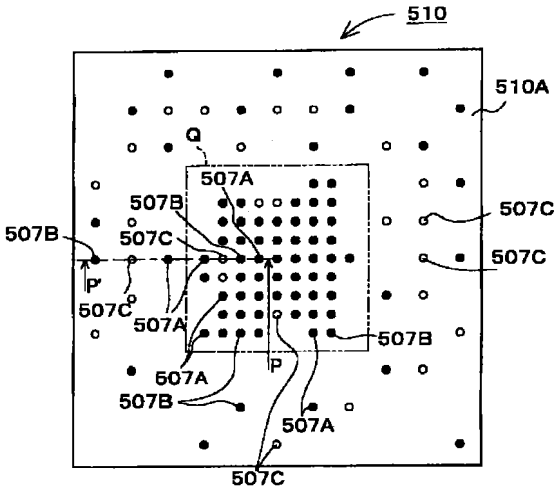

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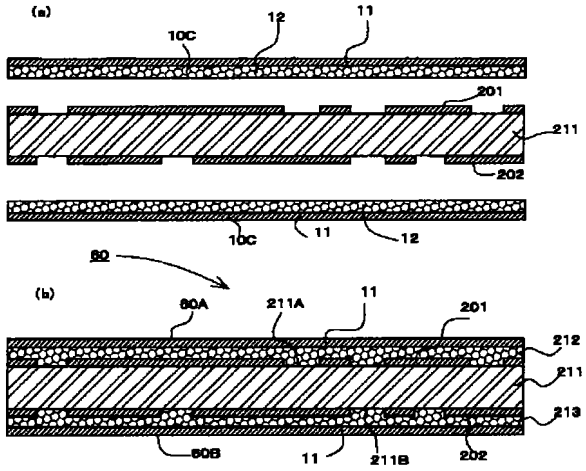
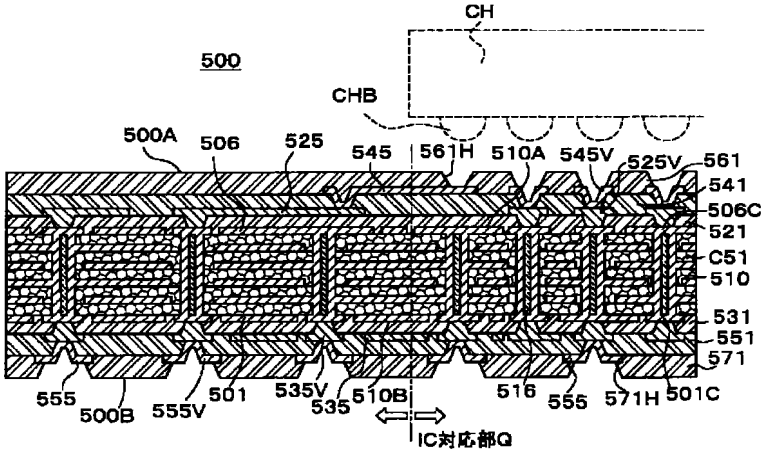


【図１１】



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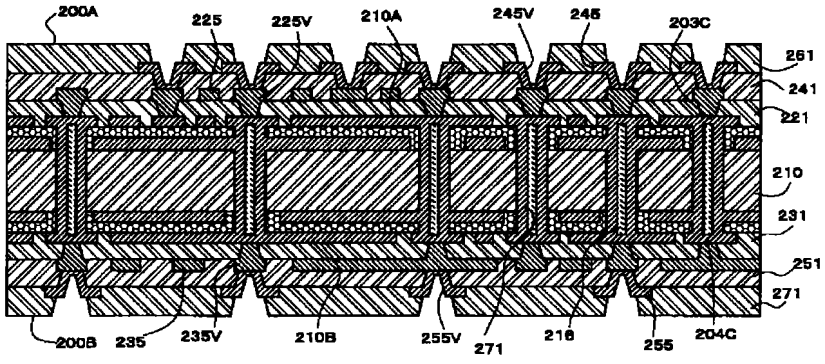

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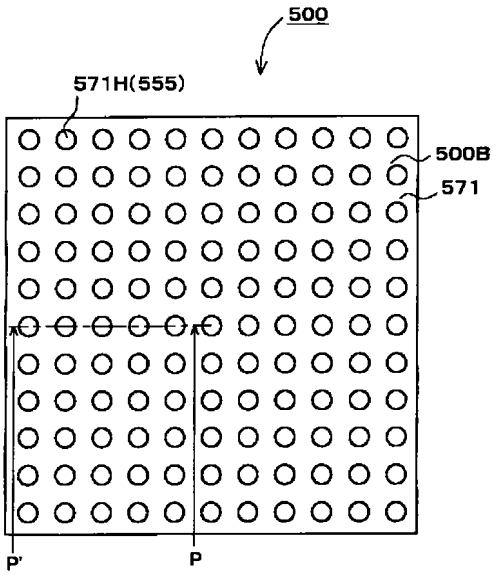

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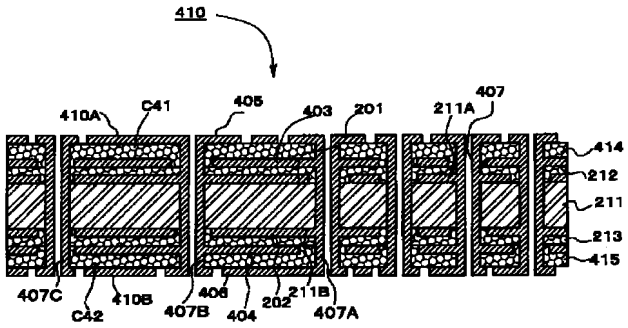

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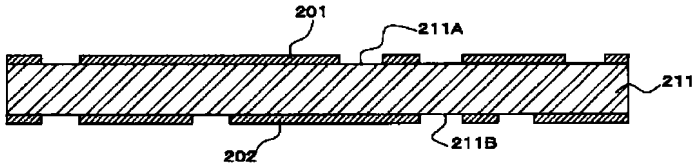

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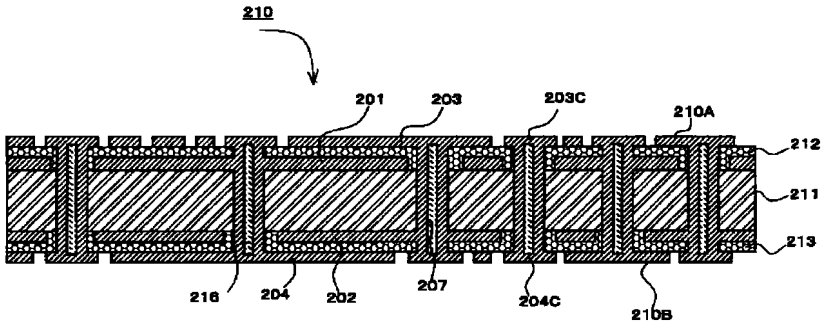

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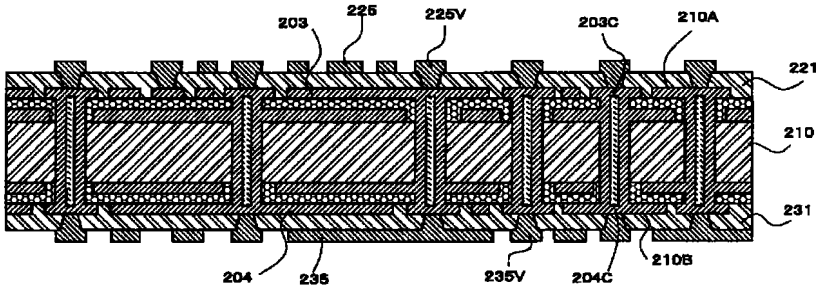
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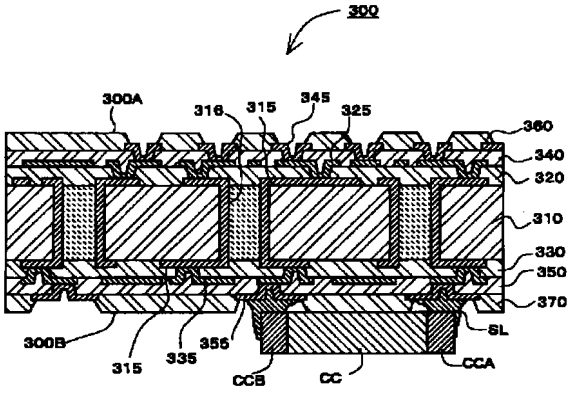
210B

【図２２】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CCA